

13

IO PORTS (Preliminary)

OVERVIEW

External interrupt pins : AppButton1 – AppButton4, JoyStick1 – Joystick5

Reset_button, Record, Toggle-up, Toggle-Down, WAKEUP1 – WAKEUP3

SD_WAKEUP, OPT_RESET, WAN1 – WAN5

: level /edge

: INTC Pending : AppButton1 – AppButton4, Record,

WAKEUP1 – WAKEUP3, SD_WAKEUP

: GPIO Pending : JoyStick1 – JoyStic5, Toggle-Up, Toggle-Down, OPT_RESET

WAN1 – WAN5, Reset_Button

Wakeup pins : AppButton1 ~ AppButton4, Record, WAKEUP1 – WAKUP3

SD_WAKEUP, **WAN5**

: level only

Debounce pins : AppButton1 – ABppButton4, JoyStick1 – Joystic5, Reset_Button,

ToggleUp, ToggleDown, SD_WAKEUP

Port A : 20 pin : AppButton 1 – 4, JoyStick1 – 5 , Toggle UP, Toggle Down, WAKEUP1 – 3, SD WAKEUP

OPT_ON, OPT_RESET, UARTCLK

Port B : 17 pin : PWR0 – 7, CTS0, CTS1, RTS0, RTS1, WAN1 – WAN5

Port C : 2 pin : Flash WE#, Flash VPEN,

Port D : 8 pin : FCD_data0 – FCD_data7

Port E : 3 pin : FCD_RST, FCD_PCLK, FCD_TPE (output only)

1 wire control : Whether APPB1, APPB4, Reset_Button are all “0” at the same time or nRESET is “0”, and then DQ goes “0” .

EXPANSION PACK Control : If GPA18 (OPT_ON) is selected, OPT_ON# signal will be out internally.

OPT_ON# is set by PA[18] port value as it is. If port is not selected with OPT_ON, OPT_ON# is sustained as "1".

EXPANSION PACK enable

- . enable1 = ~BATT_FLT & ~OPT_ON# & POWER_En
- . enable2 = (~CARD_SCKT0# | ~CARD_SCKT1#) & enable1
- . enable3 = (~CS4# | ~CS3# | ~CS2#) & enable1

Expansion Pack Signals are grouped by Enable signal.

enable1 : MCS[4:2], RD/WR# , RDY

enable2 : MPSKTSEL, PCM_CE[2:1]#, PCM_OE#, PCM_WE#, PCM_REG#, PCM_IORD#,
PCM_IOWR#,

enable3 : MDQM[3:0]#, MWE, MOE#

I/O PORT CONTROL REGISTER**PORT A CONTROL REGISTERS (PACON, PADAT, PAUP)**

Register	address	R/W	Description	Reset Value
GPA_CON1	0x000c_0000	R/W	Configures 1 the pins of port A	0xaaaaaaaa
GPA_CON2	0x000c_0004	R/W	Congigures 2 the pins of port A	0x2a
GPA_DAT	0x000c_0008	R/W	The data register for port A	0x0
GPA_UP	0x000c_000c	R/W	Pullup Disable Register	0x00080000

GPACON1	Bit	Description
GPA[0]	[1:0]	00 = GPIO Input 10 = AppButton1 (in) 01 = GPIO output 11 = reserved
GPA[1]	[3:2]	00 = GPIO Input 10 = AppButton2 (in) 01 = GPIO output 11 = reserved
GPA[2]	[5:4]	00 = GPIO Input 10 = AppButton3 (in) 01 = GPIO output 10 = reserved
GPA[3]	[7:6]	00 = GPIO Input 10 = AppButton4 (in) 01 = GPIO output 11 = reserved
GPA[4]	[9:8]	00 = input 10 = Joystic1 (in) 01 = GPIO output 11 = reserved
GPA[5]	[11:10]	00 = input 10 = Joystic2 (in) 01 = GPIO output 11 = reserved
GPA[6]	[13:12]	00 = input 10 = Joystic3 (in) 01 = GPIO output 11 = reserved
GPA[7]	[15:14]	00 = input 10 = Joystic4 (in) 01 = GPIO output 11 = reserved
GPA[8]	[17:16]	00 = input 10 = Joystic5 (in) 01 = GPIO output 11 = reserved
GPA[9]	[19:18]	00 = input 10 = ToggleUP (in) 01 = GPIO output 11 = reserved
GPA[10]	[21:20]	00 = input 10 = Toggle Down (in) 01 = GPIO output 11 = reserved
GPA[11]	[23:22]	00 = GPIO input 10 = Reset_Button (in) 01 = GPIO output 11 = reserved
GPA[12]	[25:24]	00 = GPIO input 10 = Record(in) 01 = GPIO output 11 = reserved
GPA[13]	[27:26]	00 = GPIO input 10 = WAKEUP1 (in) 01 = GPIO output 11 = reserved
GPA[14]	[29:28]	00 = GPIO input 10 = WAKEUP2 (in) 01 = GPIO output 11 = reserved
GPA[15]	[31:30]	00 = GPIO input 10 = WAKEUP3 (in) 01 = GPIO output 11 = reserved

GPA CON2	Bit	Description	
GPA[16]	[1:0]	00 = GPIO input 10 = SD_WAKEUP (in)	01 = GPIO output 11 = reserved
GPA[17]	[3:2]	00 = GPIO input 10 = OPT_ON (out)	01 = GPIO output 11 = reserved
GPA[18]	[5:4]	00 = input (OPT_RESET) 10 = OPT_RESET (in)	01 = GPIO output 11 = reserved
GPA[19]	[7:6]	00 = GPIO input 10 = UARTCLK (in)	01 = GPIO output 11 = reserved

PADAT	Bit	Description
GPA[19:0]	[19:0]	When the port is configured as input port, the corresponding bit is the pin state. When the port is configured as output port, the pin state is the same as the corresponding bit. When the port is configured as functional pin, the undefined value will be read.

PAUP	Bit	Description
GPA[19:0]	[19:0]	0: the pull up function attached to to the corresponding port pin is enabled. 1: the pull up function is disabled.

NOTE : If OPT_ON is not selected, GPADAT[18] value will be out externally and OPT_ON# signal is generated internally at the same tim. If OPT_ON# is not selected, OPT_ON# is always " 1" . (Refer to EXPANSION PACK enable signal)

PORT B CONTROL REGISTERS (PBCON, PBDAT, PBUP)

Register	address	R/W	Description	Reset Value
GPB_CON	0x000c_0010	R/W	Configures the pins of port B	0x02a900ff
GPB_DAT	0x000c_0014	R/W	The data register for port B	0x0
GPB_UP	0x000c_0018	R/W	Pullup Disable Register	0x0001e0ff

GPBCON	Bit	Description	
GPB[0]	[0]	0 = input	1 = output (PWR0)
GPB[1]	[1]	0 = input	1 = output (PWR1)
GPB[2]	[2]	0 = input	1 = output (PWR2)
GPB[3]	[3]	0 = input	1 = output (PWR3)
GPB[4]	[4]	0 = input	1 = output (PWR4)
GPB[5]	[5]	0 = input	1 = output (PWR5)
GPB[6]	[6]	0 = input	1 = output (PWR6)
GPB[7]	[7]	0 = input	1 = output (PWR7)
GPB[8]	[9:8]	00 = input 10 = CTS0 (input)	01 = output 11 = CK16MOUT
GPB[9]	[11:10]	00= input 10= RTS0 (output)	01 = output 11 = CK48MOUT
GPB[10]	[13:12]	00 = input 10 = CTS1 (input)	01 = output 11 = reversed
GPB[11]	[15:14]	00= input 10= RTS1 (output)	01 = output 11 = reserved
GPB[12]	[17:16]	0 0= input 10=WAN1 (in)	01 = output 11=reserved
GPB[13]	[19:18]	0 0= input 10=WAN2 (in)	01 = output 11=reserved
GPB[14]	[21:20]	0 0= input 10=WAN3 (in)	01 = output 11=reserved
GPB[15]	[23:22]	0 0= input 10=WAN4 (in)	01 = output 11=reserved
GPB[16]	[25:24]	0 0= input 10=WAN5 (in)	01 = output 11=reserved

PBDAT	Bit	Description
PB[16:0]	[16:0]	When the port is configured as input port, the corresponding bit is the pin state. When the port is configured as output port, the pin state is the same as the corresponding bit. When the port is configured as functional pin, the undefined value will be read.

PBUP	Bit	Description
PB[16:0]	[16:0]	0: the pull up function attached to to the corresponding port pin is enabled. 1: the pull up function is disabled.

NOTE : 1. WAKEUP function is added to WAN5.
2. CK16OUT is added to GPB8.
3. CK48OUT is added to GPB9.

PORT C CONTROL REGISTERS (PCCON, PCDAT, PCUP)

Register	address	R/W	Description	Reset Value
GPC_CON	0x000c_001c	R/W	Configures the pins of port C	0x00000065
GPC_DAT	0x000c_0020	R/W	The data register for port C	0x2
GPC_UP	0x000c_0024	R/W	Pullup Disable Register	0x00000003

PCCON	Bit	Description
PC[0]	[0]	0 = input 1 = output (Flash VPEN)
PC[1]	[2:1]	00 = input 01 = output 10 = Flash WE # 11 = reserved
FWE_EN	[4]	Flash WE# Enable. This bit is valid when PC[1] is set Flash WE#. 0 = disable (pass through WE#) 1= enable
FWE_16	[5]	Flash bus width 0 = 16bit 1=32bit
FWE_size	[7:6]	Flash Memory Size 00 = 64Mbit 01 = 128 Mbit 10 = 256Mbit 11 = 512Mbit

PCDAT	Bit	Description
PC[1:0]	[1:0]	When the port is configured as input port, the corresponding bit is the pin state. When the port is configured as output port, the pin state is the same as the corresponding bit. When the port is configured as functional pin, the undefined value will be read.

PCUP	Bit	Description
PC[1:0]	[1:0]	0: the pull up function attached to to the corresponding port pin is enabled. 1: the pull up function is disabled.

PORT D CONTROL REGISTERS (PDCONPDUP)

Register	address	R/W	Description	Reset Value
GPD_CON	0x000c_0028	R/W	Configures the pins of port D	0x0000aaaa
GPD_DAT	0x000c_002c	R/W	The data register for port D	0x0
GPD_UP	0x000c_0030	R/W	Pullup Disable Register	0x00

PDCON	Bit	Description
PD[0]	[1:0]	0 = input [n] 01 = output 10 = FCD_Data[0] (in) 11 = reserved
PD[1]	[3:2]	0 = input [n] 01 = output 10 = FCD_Data[1] (in) 11 = reserved
PD[2]	[5:4]	0 = input [n] 01 = output 10 = FCD_Data[2] (in) 11 = reserved
PD[3]	[7:6]	0 = input [n] 01 = output 10 = FCD_Data[3] (in) 11 = reserved
PD[4]	[9:8]	0 = input [n] 01 = output 10 = FCD_Data[4] (in) 11 = reserved
PD[5]	[11:10]	0 = input [n] 01 = output 10 = FCD_Data[5] (in) 11 = reserved
PD[6]	[13:12]	0 = input [n] 01 = output 10 = FCD_Data[6] (in) 11 = reserved
PD[7]	[15:14]	0 = input [n] 01 = output 10 = FCD_Data[7] (in) 11 = reserved

PCDAT	Bit	Description
PD[7:0]	[7:0]	When the port is configured as input port, the corresponding bit is the pin state. When the port is configured as FCD_data, the pin state transfer to FCD Controller.

PDUP	Bit	Description
PD[1:0]	[7:0]	0: the pull up function attached to to the corresponding port pin is enabled. 1: the pull up function is disabled.

PORT E CONTROL REGISTERS (PECON,PEDAT)

Register	address	R/W	Description	Reset Value
GPE_CON	0x000c_0034	R/W	Configures the pins of port E	0x00000007
GPE_DAT	0x000c_0038	W	The data register for port E	0x0

PECON	Bit	Description
PE[0]	[0]	0 = output 1 = FCD_RST
PE[1]	[1]	0 = output 1 = FCD_PCLK
PE[2]	[2]	0 = output 1 = FCD_TPE

PEDAT	Bit	Description
PE[2:0]	[2:0]	When the port is configured as output port, the pin state is the same as the corresponding bit. When the port is configured as functional pin, the undefined value will be read

8M CLOCK OUT CONTROL REGISTERS (CK8MCON)

Register	address	R/W	Description	Reset Value
CK8MCON	0x000c_003c	R/W	Configures the pins of port E	0x00000000

CK8MCON	Bit	Description
CK8MEN	[0]	8M Clock Out Enable 0 = CK8M disable 1 = CK8M enable
CK8MselCK	[1]	Select CK8M source clock 0 = PCLK 1 = USBCLK
reserved	[3:2]	reserved
CK8MDIV	[7:4]	CK8M Divide value Clock period (CLK/(CK8MDIV+1))
CK8MCMP	[11:8]	CK8M Compare value Clock toggle value. (< CK8MDIV)
CKOUTSEL	[13:12]	CKOUT8M output select 00 : CKOUT8M 01 : UPLL_out 10 : UCLK 11 : HCLK
reserved	[15:14]	reserved
CK16MEN	[16]	16M Clock Out Enable 0 = CK 16M disable 1 = CK 16M enable
CK16MselCK	[17]	Select CK16M source clock 0 = PCLK 1 = USBCLK
reserved	[19:18]	reserved
CK16MSEL	[21:20]	Select CK16M output select 00 : bypass CLK 01 : CLK/2 10 : CLK/3 11 : CLK/4
reserved	[23:22]	reserved
CK48MEN	[24]	48M Clock Out Enable 0 = CK 48M disable 1 = CK 48M
CK48MselCK	[25]	Select CK48M source clock 0 = PCLK 1 = USBCLK
reserved	[27:26]	reserved
CK48MSEL	[29:28]	Select CK48M output select 00 : bypass CLK 01 : CLK/2 10 : CLK/3 11 : CLK/4
reserved	[31:30]	reserved

SPECIAL PORT CONTROL REGISTER (SPCR)

Register	address	R/W	Description	Reset Value
SPCR	0x000c_0040	R/W	Special Port control	0x00000000

SPCR	Bit	Description
SPUCR	[7:0]	Data port Pull up Control register [0] : MD[7:0] Pull up enable [1] : MD[15:8] Pull up enable [2] : MD[23:16] Pull up enable [3] : MD[31:24] Pull up enable [4] : D[7:0] Pull up enable [5] : D[15:8] Pull up enable [6] : D[23:16] Pull up enable [7] : D[31:24] Pull up enable 0 = enable 1 = disable
USBSUSPEND	[9:8]	USB Pad Suspend mode [8] : USB Port [0] suspend enable [9] : USB port [1] suspend enable 0 = suspend enable 1= suspend disable
SDPUCR	[10]	SD Card Data Pull up control SD[3:0] : pull up enable 0 = enable 1=disable

GPIO INTERRUPT REGISTER 1 (GPIOINT1)

Register	address	R/W	Description	Reset Value
GPIOINT1	0x000c_0044	R/W	GPIO interrupt level	0x00000000

GPIOINT1	Bit	Description
APPB1INT	[2:0]	AppButton1 interrupt level when GPA[0] is set AppButton1 000 = Low level 001= high level 010 = rising edge 011=falling edge 11x = both edge
APPB1FLT	[3]	AppButton1 Filter Enable 0 = Filter Disable 1= Filter Enable
APPB2INT	[6:4]	AppButton2 interrupt level when GPA[1] is set AppButton2 000 = Low level 001= high level 01x = rising edge 10x=falling edge 11x = both edge
APPB2FLT	[7]	AppButton2 Filter Enable 0 = Filter Disable 1= Filter Enable
APPB3INT	[10:8]	AppButton3 interrupt level when GPA[2] is set AppButton3 000 = Low level 001= high level 01x = rising edge 10x=falling edge 11x = both edge
APPB3FLT	[11]	AppButton3 Filter Enable 0 = Filter Disable 1= Filter Enable
APPB4INT	[14:12]	AppButton4 interrupt level when GPA[3] is set AppButton4 000 = Low level 001= high level 01x = rising edge 10x=falling edge 11x = both edge
APPB4FLT	[15]	AppButton4 Filter Enable 0 = Filter Disable 1= Filter Enable
JOYSTICK1INT	[18:16]	JOYSTICK1 interrupt level when GPA[4] is set JOYSTICK1 000 = Low level 001= high level 01x = rising edge 10x=falling edge 11x = both edge
JOYSTICK1FLT	[19]	JOYSTICK1 Filter Enable 0 = Filter Disable 1= Filter Enable
JOYSTICK2INT	[22:20]	JOYSTICK2 interrupt level when GPA[5] is set JOYSTICK2 000 = Low level 001= high level 01x = rising edge 10x=falling edge 11x = both edge
JOYSTICK2FLT	[23]	JOYSTICK2 Filter Enable 0 = Filter Disable 1= Filter Enable

JOYSTICK3INT	[26:24]	JOYSTICK2 interrupt level when GPA[6] is set JOYSTICK3 000 = Low level 001= high level 01x = rising edge 10x=falling edge 11x = both edge
JOYSTICK3FLT	[27]	JOYSTICK3 Filter Enable 0 = Filter Disable 1= Filter Enable
JOYSTICK4INT	[30:28]	JOYSTICK4 interrupt level when GPA[7] is set JOYSTICK4 000 = Low level 001= high level 01x = rising edge 10x=falling edge 11x = both edge
JOYSTICK4FLT	[31]	JOYSTICK4 Filter Enable 0 = Filter Disable 1= Filter Enable

GPIO INTERRUPT REGISTER 2 (GPIOINT2)

Register	address	R/W	Description	Reset Value
GPIOINT2	0x000c_0048	R/W	GPIO interrupt level	0x00000000

GPIOINT2	Bit	Description
JOYSTICK5INT	[2:0]	JOYSTICK4 interrupt level when GPA[8] is set JOYSTICK9 000 = Low level 001= high level 01x = rising edge 10x=falling edge 11x = both edge
JOYSTICK5FLT	[3]	JOYSTICK4 Filter Enable 0 = Filter Disable 1= Filter Enable
ToggleUPINT	[6:4]	ToggleUP Interrupt level when GPA[9] is set ToggleUP 000 = Low level 001= high level 01x = rising edge 10x=falling edge 11x = both edge
ToggleUPFLT	[7]	ToggleUP Fileter Enable 0 = Filter Disable 1= Filter Enable
ToggleDownINT	[10:8]	ToggleDown Interrupt level when GPA[10] is set ToggleUP 000 = Low level 001= high level 01x = rising edge 10x=falling edge 11x = both edge
ToggleDownFLT	[11]	ToggleDown Filter Enable 0 = Filter Disable 1= Filter Enable
Reset_ButINT	[14:12]	Reset Button Interrupt level when GPA[11] is set Reset_Button 000 = Low level 001= high level 01x = rising edge 10x=falling edge 11x = both edge
Reset_ButtonFLT	[15]	Reset_Button Filter Enable 0 = Filter Disable 1= Filter Enable
RecordINT	[18:16]	Record Interrupt level when GPA[12] is set Record 000 = Low level 001= high level 01x = rising edge 10x=falling edge 11x = both edge
reserved	[19]	Reserved
WAKEUP1INT	[22:20]	WAKEUP1 interrupt level when GPA[0] is set WAKEUP1 000 = Low level 001= high level 01x = rising edge 10x=falling edge 11x = both edge
Reserved	[23]	Must be "0"
WAKEUP2INT	[26:24]	WAKEUP2 interrupt level when GPA[0] is set WAKEUP2 000 = Low level 001= high level 01x = rising edge 10x=falling edge 11x = both edge
Reserved	[27]	Must be "0"

WAKEUP3INT	[30:28]	WAKEUP3 interrupt level when GPA[0] is set WAKEUP3 000 = Low level 001= high level 01x = rising edge 10x=falling edge 11x = both edge
Reserved	[31]	Must be "0"

GPIO INTERRUPT REGISTER 3 (GPIOINT3)

Register	address	R/W	Description	Reset Value
GPIOINT3	0x000c_004c	R/W	GPIO interrupt level	0x00000000

GPIOINT3	Bit	Description
SD_WAKEUPINT	[2:0]	SD_WAKEUP interrupt level when GPA[16] is set SD_WAKEUP 000 = Low level 001= high level 01x = rising edge 10x=falling edge 11x = both edge
SD_WAKEUPFLT	[3]	SD_WAKEUP Filter Enable 0 = Filter Disable 1= Filter Enable
OPT_ResetINT	[6:4]	OPT RESET interrupt level when GPA[18] is set OPT_RESET 000 = Low level 001= high level 01x = rising edge 10x=falling edge 11x = both edge
reserved	[7]	Reserved
WAN1INT	[10:8]	WAN1 interrupt level when GPB[12] is set WAN1 000 = Low level 001= high level 01x = rising edge 10x=falling edge 11x = both edge
Reserved	[11]	Reserved
WAN2INT	[14:12]	WAN2 interrupt level when GPB[13] is set WAN2 000 = Low level 001= high level 01x = rising edge 10x=falling edge 11x = both edge
Reserved	[15]	Reserved
WAN3INT	[18:16]	WAN3 interrupt level when GPB[14] is set WAN3 000 = Low level 001= high level 01x = rising edge 10x=falling edge 11x = both edge
Reserved	[19]	Reserved
WAN4INT	[22:20]	WAN4 interrupt level when GPB[15] is set WAN4 000 = Low level 001= high level 01x = rising edge 10x=falling edge 11x = both edge
reserved	[23]	Reserved
WAN5INT	[26:24]	WAN5 interrupt level when GPB[16] is set WAN5 000 = Low level 001= high level 01x = rising edge 10x=falling edge 11x = both edge
reserved	[27]	Reserved

GPIO FILTER REGISTER 4 (GPIOFLT4)

Register	Address	R/W	Description	Reset Value
GPIOFLT4	0x000c_005c	R/W	GPIO Filtering	0x00000000

GPIOFLT4	Bit	Description
WID_JOYST2	[13:0]	Filtering width of JOYSTICK2
Reserved	[15:14]	Must be "0"
WID_JOYST3	[29:16]	Filtering width of JOYSTICK3
Reserved	[31:30]	Must be "0"

GPIO FILTER REGISTER 5 (GPIOFLT5)

Register	Address	R/W	Description	Reset Value
GPIOFLT5	0x000c_0060	R/W	GPIO Filtering	0x00000000

GPIOFLT5	Bit	Description
WID_JOYST4	[13:0]	Filtering width of JOYSTICK4
Reserved	[15:14]	Must be "0"
WID_JOYST5	[29:16]	Filtering width of JOYSTICK5
Reserved	[31:30]	Must be "0"

GPIO FILTER REGISTER 6 (GPIOFLT6)

Register	Address	R/W	Description	Reset Value
GPIOFLT6	0x000c_0064	R/W	GPIO Filtering	0x00000000

GPIOFLT6	Bit	Description
WID_TOGUP	[13:0]	Filtering width of ToggleUP
Reserved	[15:14]	Must be "0"
WID_TOGDN	[29:16]	Filtering width of ToggleDown
Reserved	[31:30]	Must be "0"

GPIO FILTER REGISTER 7 (GPIOFLT7)

Register	Address	R/W	Description	Reset Value
GPIOFLT7	0x000c_0068	R/W	GPIO Filtering	0x00000000

GPIOFLT7	Bit	Description
WID_RstBut	[13:0]	Filtering width of Reset Button
Reserved	[15:14]	Must be "0"
WID_SDWAKE	[29:16]	Filtering width of SD WAKEUP
Reserved	[31:30]	Must be "0"

GPIO MONITOR REGISTER (GPIOMON)

Register	Address	R/W	Description	Reset Value
GPIOMON	0x000c_006c	R	Monitor GPIO filtering signals	0x00000000

GPIOMON	Bit	Description
MON_APPB1	[0]	AppButton1 signal after filtering
MON_APPB2	[1]	AppButton2 signal after filtering
MON_APPB3	[2]	AppButton3 signal after filtering
MON_APPB4	[3]	AppButton4 signal after filtering
MON_JOY1	[4]	JOYSTICT1 signal after filtering
MON_JOY2	[5]	JOYSTICT2 signal after filtering
MON_JOY3	[6]	JOYSTICT3 signal after filtering
MON_JOY4	[7]	JOYSTICT4 signal after filtering
MON_JOY5	[8]	JOYSTICT5 signal after filtering
MON_TOGUP	[9]	Toggle UP signal after filtering
MON_TOGDN	[10]	Toggle Down signal after filtering
MON_RSTBUT	[11]	Reset Button signal after filtering
MON_SDWAKE	[12]	SD_WAKUP signal after filtering

GPIO INTERRUPT ENABLE REGISTER (GPIOENINT1)

Register	Address	R/W	Description	Reset Value
GPIOENINT1	0x000c_0070	R/W	GPIO Pending register	0x00000000

GPIOENINT1	Bit	Description
EN_APPB1	[0]	Interrupt enable of AppButton1 0 = disable 1= enable
EN_APPB2	[1]	Interrupt enable of AppButton2 0 = disable 1= enable
EN_APPB3	[2]	Interrupt enable of AppButton3 0 = disable 1= enable
EN_APPB4	[3]	Interrupt enable of AppButton4 0 = disable 1= enable
EN_RECORD	[4]	Interrupt enable of Record 0 = disable 1= enable
EN_WAKEUP1	[5]	Interrupt enable of WAKEUP 1 0 = disable 1= enable
EN_WAKEUP1	[6]	Interrupt enable of WAKEUP 2 0 = disable 1= enable
EN_WAKEUP1	[7]	Interrupt enable of WAKEUP 3 0 = disable 1= enable
EN_SDWAKE	[8]	Interrupt enable of SD WAKE UP 0 = disable 1= enable

GPIO INTERRUPT ENABLE REGISTER (GPIOENINT2)

Register	Address	R/W	Description	Reset Value
GPIOENINT2	0x000c_0074	R/W	GPIO Pending register	0x00000000

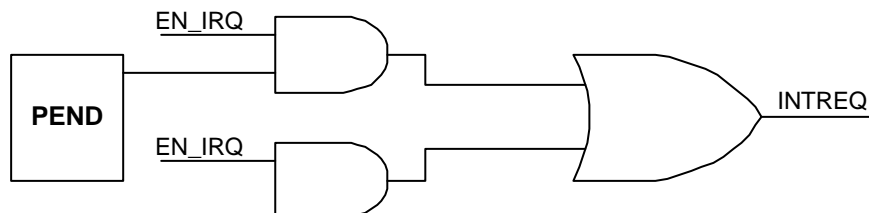
GPIOENINT2	Bit	Description
EN_JOYSTICK1	[0]	Interrupt enable of Joystick 1 0 = disable 1= enable
EN_JOYSTICK2	[1]	Interrupt enable of Joystick 2 0 = disable 1= enable
EN_JOYSTICK3	[2]	Interrupt enable of Joystick 3 0 = disable 1= enable
EN_JOYSTICK4	[3]	Interrupt enable of Joystick 4 0 = disable 1= enable
EN_JOYSTICK5	[4]	Interrupt enable of Joystick 5 0 = disable 1= enable
EN_ToggleUP	[5]	Interrupt enable of Toggle UP 0 = disable 1= enable
EN_ToggleDN	[6]	Interrupt enable of Toggle Down 0 = disable 1= enable
EN_RstBut	[7]	Interrupt enable of Reset Button 0 = disable 1= enable
EN_OPT_RESET	[8]	Interrupt enable of OPT_RESET 0 = disable 1= enable
EN_WAN1	[9]	Interrupt enable of WAN1 0 = disable 1= enable
EN_WAN2	[10]	Interrupt enable of WAN2 0 = disable 1= enable
EN_WAN3	[11]	Interrupt enable of WAN3 0 = disable 1= enable
EN_WAN4	[12]	Interrupt enable of WAN4 0 = disable 1= enable
EN_WAN5	[13]	Interrupt enable of WAN5 0 = disable 1= enable

GPIO INTERRUPT PENDING Register (GPIOPEND)

Register	Address	R/W	Description	Reset Value
GPIOPEND	0x000c_0078	R/W	GPIO Pending register	0x00000000

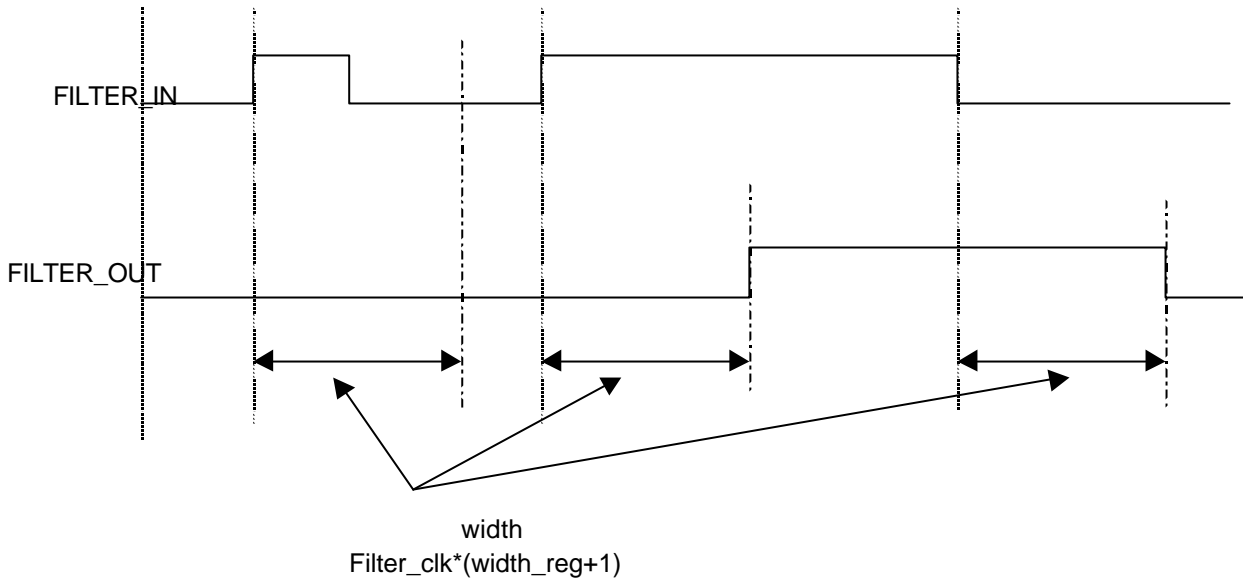
GPIOPEND	Bit	Description
JOYSTICK1	[0]	Interrupt Pended when GPA[4] is set Joystick 1 0 = not occur 1= occur It' s cleared by writing " 1" .
JOYSTICK2	[1]	Interrupt Pended when GPA[5] is set Joystick 2 0 = not occur 1= occur
JOYSTICK3	[2]	Interrupt Pended when GPA[6] is set Joystick 3 0 = not occur 1= occur
JOYSTICK4	[3]	Interrupt Pended when GPA[7] is set Joystick 4 0 = not occur 1= occur
JOYSTICK5	[4]	Interrupt Pended when GPA[8] is set Joystick 5 0 = not occur 1= occur
ToggleUP	[5]	Interrupt Pended when GPA[9] is set Toggle Up 0 = not occur 1= occur
ToggleDN	[6]	Interrupt Pended when GPA[10] is set Toggle Down 0 = not occur 1= occur
RstBut	[7]	Interrupt Pended when GPA[11] is set Reset Button 0 = not occur 1= occur
OPT_RESET	[8]	Interrupt Pended when GPA[18] is set OPT_RESET 0 = not occur 1= occur
WAN1	[9]	Interrupt Pended when GPB[12] is set WAN1 0 = not occur 1= occur
WAN2	[10]	Interrupt Pended when GPB[13] is set WAN2 0 = not occur 1= occur
WAN3	[11]	Interrupt Pended when GPB[14] is set WAN3 0 = not occur 1= occur
WAN4	[12]	Interrupt Pended when GPB[15] is set WAN4 0 = not occur 1= occur
WAN5	[13]	Interrupt Pended when GPB[16] is set WAN5 0 = not occur 1= occur

NOTE: When the appropriate GPIOENINT bit was set, this register can make interrupt signal sent to INTC. Pending register can be pending only when the appropriate bit was selected.



- FILTER : AppButton1, AppButton2, AppButton3, AppButton4, JoyStick1, JoyStick2, JoyStick3, Joystick4,

JoyStick5, ToggleUP, ToggleDown, Reset_Button, SD_WAKEUP



- 8M Clock Out Setting

