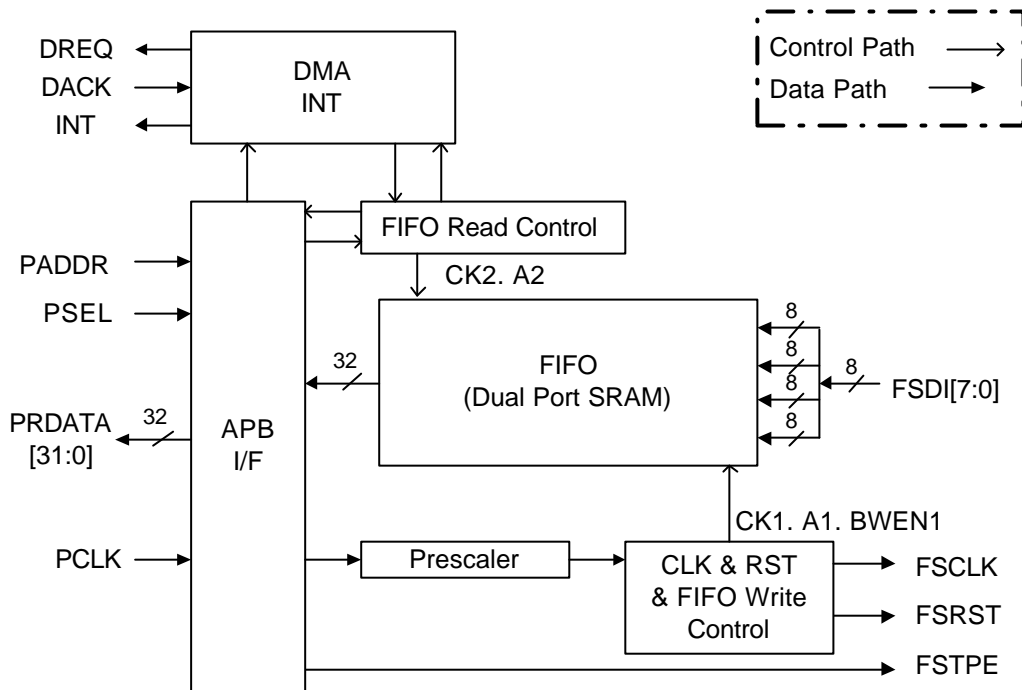


# 8 FSI(Fingerprint Sensor Interface)(Preliminary)

## BLOCK DIAGRAM



## BASIC FEATURES

- 8bit prescaling : Baud Rate = PCLK / (2 ~ 512)
- FSDI[7:0] 1byte read, PRDATA[31:0] 1word(32bit) read
- When PCLK is 50Mhz and FSCLK is 2 Mhz, the bandwidth is 100 times.
- Polling, Interrupt, and DMA Operation
- FIFO size : 1124 byte
- 1124 counter and Dummy integration time counter are included.

## FSI OPERATION

A serial clock line synchronizes sampling of the information on the FSDI[7:0] data lines. The transmission frequency is controlled by making the appropriate bit settings to the FSIPRE register. You can modify its frequency to adjust the baud rate data register value.

### Programming Procedure

To program the FSI modules, follow these basic steps :

1. Set FSIPRE to configure with a proper value.(FSCLK frequency is appropriate at 1Mhz ~ 2Mhz)
2. Set FSIDMC to configure with a proper value.(Bandwidth is appropriate at 1Mbyte/s)  
If FSCLK frequency is 2Mhz and FSIDMC value is 1124, then the bandwidth is 1Mbyte/s.
3. Set FSIFCON to configure with a proper trigger level.(You should not select the trigger level to 281 full word, if DMA mode does not operate. Because it is possible to occur the data overrun.)
4. Set FSICON to configure properly with clock & interrupt enable and CRMOD(CLK & RST Mode) bit.  
CRMOD = 2' b01 → frames receive start  
CRMOD = 2' b10 → NAP mode(the power down mode of fingerprint chip) start  
CRMOD = 2' b00 → frames receive(or NAP) stop
5. Read data from Data Register(FSIDAT) while FIFO trigger level detect(FTDET is set).
6. If you receive all frames you want, set FSICON to configure CRMOD to stop mode.
7. Confirm the end of last frame receive by auto setting of LFRM flag
8. Clear the corresponding flag of FSISTA through writing one with this bit

## FSI SPECIAL REGISTERS

### FSI Control Register(FSICON)

Register	Address	R/W	Description	Reset Value
FSICON	0X0b_0000	R/W	FSI Control Register	0x0

FSICON	Bit	Description	Initial Value
Reserved	[31:9]		
FSI Transfer Mode Select (FMODE)	[8:7]	Determines how and by what FSIDAT is read 00 = polling mode,           01 = interrupt mode 10 = DMA mode,             11 = reserved	00
LFRM Interrupt Enable (LFINT)	[6]	Determines FSI generate an interrupt if last frame receiving completes 0 = disable,                 1 = interrupt enable	0
INVL Interrupt Enable (ININT)	[5]	Determines FSI generate an interrupt if invalid data error occur 0 = disable,                 1 = interrupt enable	0
DCOL Interrupt Enable (DCINT)	[4]	Determines FSI generate an interrupt if data collision error occur 0 = disable,                 1 = interrupt enable	0
Clock Out Enable (ENCLK)	[3]	Determines whether FSCLK Out enable or not 0 = disable(prescaler off),   1 = clock enable	0
Temp Power Enable(TPE)	[2]	Determines FSTPE pin active or not. 0 = TPE low,                 1 = TPE active high	0
CLK & RST Mode Select (CRMOD)	[1:0]	Determines by what mode FSCLK & FSRST transmit to FS 00 = frame stop mode,       01 = frame start mode(1 RST) 10 = NAP mode,             11 = frame receive mode(0 RST)	00

\* **frame start mode** asserts 1 RST pulse, but **frame receive mode** doesn't assert any RST pulse. You should use **frame start mode** when you start frame(s) receiving. And, you should use **frame receive mode** when frames receiving is going on.



**FSI Baud Rate Prescaler Register(FSIPRE)**

Register	Address	R/W	Description	Reset Value
FSIPRE	0X0b_0004	R/W	FSI Baud Rate Prescaler Register	0x00

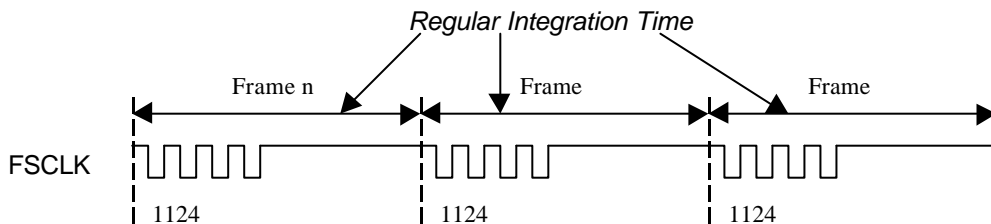
FSIPRE	Bit	Description	Initial Value
Reserved	[31:8]		
Prescaler Value	[7:0]	Determines FSI clock(FSCLK) rate as above equation. Baud rate = PCLK / 2 / (Prescaler value + 1)	0x00

**FSI Dummy Integration Time Counter Register(FSIDMC)**

Register	Address	R/W	Description	Reset Value
FSIDMC	0X0b_0008	R/W	FSI Dummy Integration Time Counter Register	0x000

FSIDMC	Bit	Description	Initial Value
Reserved	[31:12]		
Dummy Integration Time Counter	[11:0]	Counter value = 0 ~ 4095 times(by FSCLK rate)	0x000

$$Regular\ Integration\ Time = (1124 + FSIDMC\ value) / (FSCLK\ freq)$$



**FSI FIFO Control Register(FSIFCON)**

Register	Address	R/W	Description	Reset Value
FSIFCON	0X0b_000C	R/W	FSI FIFO Control Register	0x00

FSIFCON	Bit	Description	Initial Value
Reserved	[31:3]		
FIFO Trigger level (FTRIG)	[2:1]	Determines data ready trigger level of FIFO(total 281word). 00 = 1word, 01 = 70word 10 = 140word, 11 = 281word(full)	00
FIFO Reset(FRST)	[0]	Determines resetting FIFO count. 0 = normal mode, 1 = FIFO count reset	0

\* FIFO count is the difference between write pointer and read pointer of FIFO. Read pointer and FIFO count resets immediately if FSIFCON' s FRST bit sets. But **write pointer can be reset. after FSISTA' s LFRM flag is active,** because write pointer should always increase until receiving the frame fully.



**FSI Status Register(FSISTA)**

Register	Address	R/W	Description	Reset Value
FSISTA	0X0b_0010	R/(C)	FSI Status Register Register	0x0

FSISTA	Bit	Description	Initial Value
Reserved	[31:13]		
Last Frame Receive complete (LFRM)	[12] R/C	This flag is set if last frame data writing to FIFO completes. This flag is cleared by setting to one this bit. 0 = not complete, 1 = last frame complete	0
Invalid Data Receiving Error Flag(INVL)	[11] R/C	This flag is set if data receives from FIFO when FIFO is empty. This flag is cleared by setting to one this bit. 0 = not detect, 1 = invalid data error detect	0
Data Collision Error Flag(DCOL)	[10] R/C	This flag is set if another data receives from FSDI when FIFO is full. This flag is cleared by setting to one this bit. 0 = not detect, 1 = collision error detect	0
FIFO Count (FFCNT)	[9:1]	Number of data(word) in FIFO(0~281)	0x000
FIFO Trigger level Detect (FTDET)	[0]	This bit indicates that FIFO reaches trigger level. 0 = not detect, 1 = detect	0

**FSI Data Register(FSIDAT)**

Register	Address	R/W	Description	Reset Value
FSIDAT	0X0b_0014	R	FSI Data Register	0x00000000

FSIDAT	Bit	Description	Initial Value
FSI Data Register	[31:0]	This field contains the data to be received over the FSI channel	0x00000000

