

# 4 EXPANSION PACK INTERFACE (Preliminary)

## OVERVIEW

The electrical connection between the main unit and the expansion pack includes pins for two PCMCIA/CF devices, a 16/32-bit static memory/I/O interface, battery expansion, and other miscellaneous functions. The interface leverages the capability of the processor in the main unit. Figure 1 (Block Diagram) and Figure 2 (Expansion Pack Interface on Expansion Pack) show block diagrams of the interface on the main unit and a possible implementation of an expansion pack, respectively.

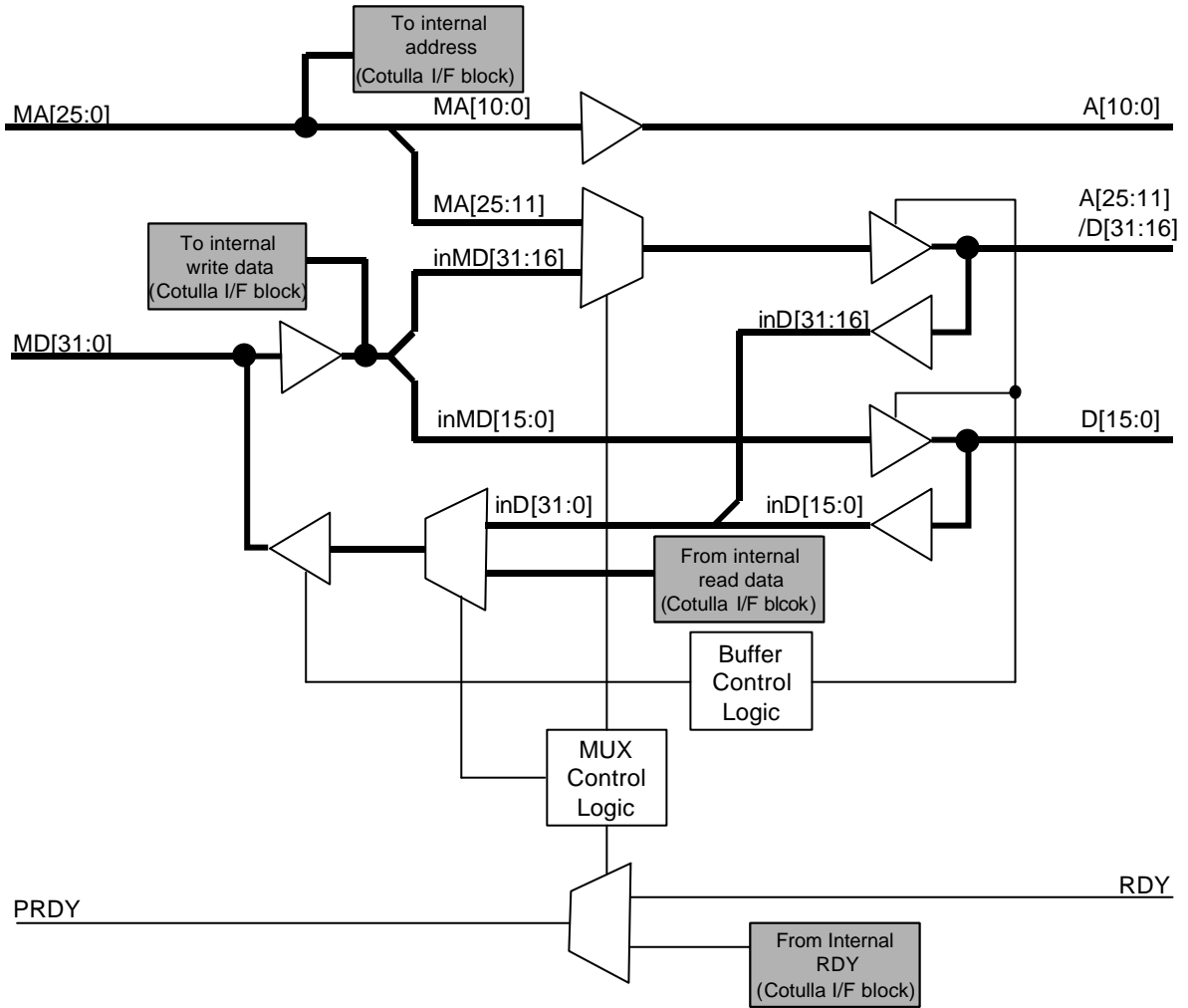
The address, data and control signals from the processor are connected to the expansion pack through isolation buffers. The isolation buffers are tri-stated when the system is in idle mode or not accessing the expansion pack. It is recommended that the expansion pack handle the tri-stating bus without excessive current draw (one recommendation is to include light pull-down or pull-up resistors on the signals). The address bus, A[25:0] and data bus, D[31:0], are used for parallel interfacing to PCMCIA/CF, static memory and I/O devices.

The various control signals for PCMCIA/CF, static memory and I/O enable different functions on the expansion pack. A portion of the address bus, A[25: 11], is multiplexed with most of the upper bytes of the data bus, D[30:16], to provide a 32-bit data bus interface. The 32-bit interface can perform these accesses only with an 11-bit address.

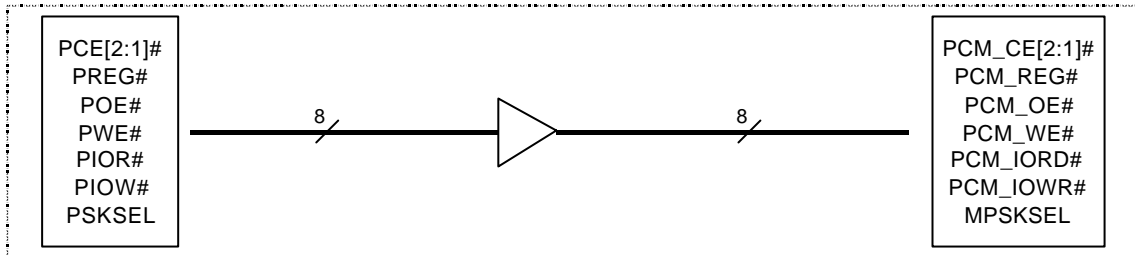
The 32-bit data bus capability provides faster access for expansion packs that require high data throughput. Typically, the interface accesses 16-bit data with a 26-bit address bus. The expansion pack interface supports two PCMCIA/CF devices in the expansion pack. If an expansion pack has two PCMCIA or CF devices, it must include buffers and control logic to isolate the signals.

### EXPANSION PACK INTERFACE OPERATION

FIGURE 1. BLOCK DIAGRAM



*PCMCIA Control signals*



*Memory or I/O Control signals*

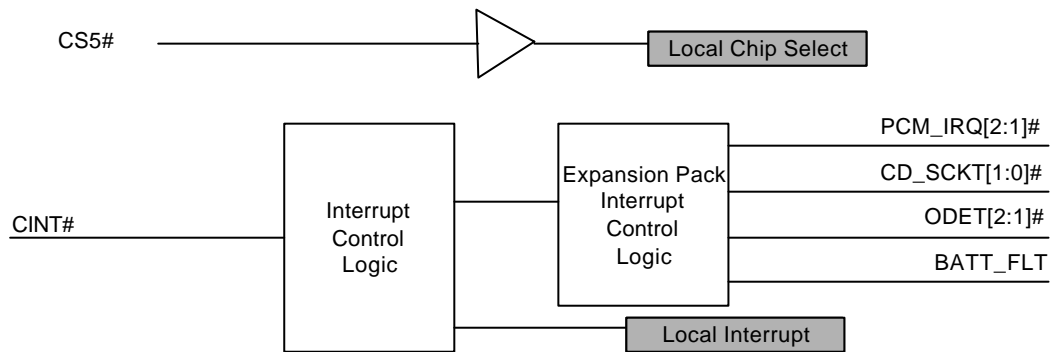
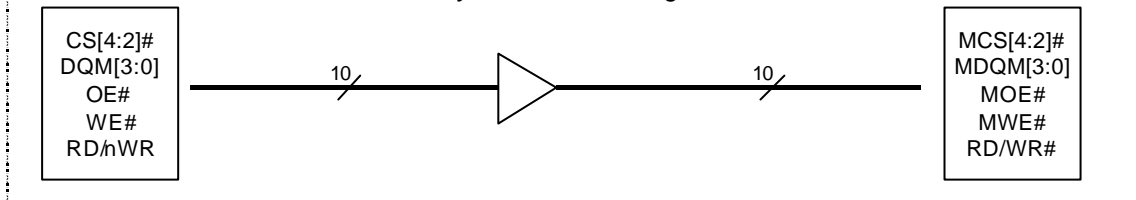


FIGURE 2. EXPANSION PACK INTERFACE ON EXPANSION PACK

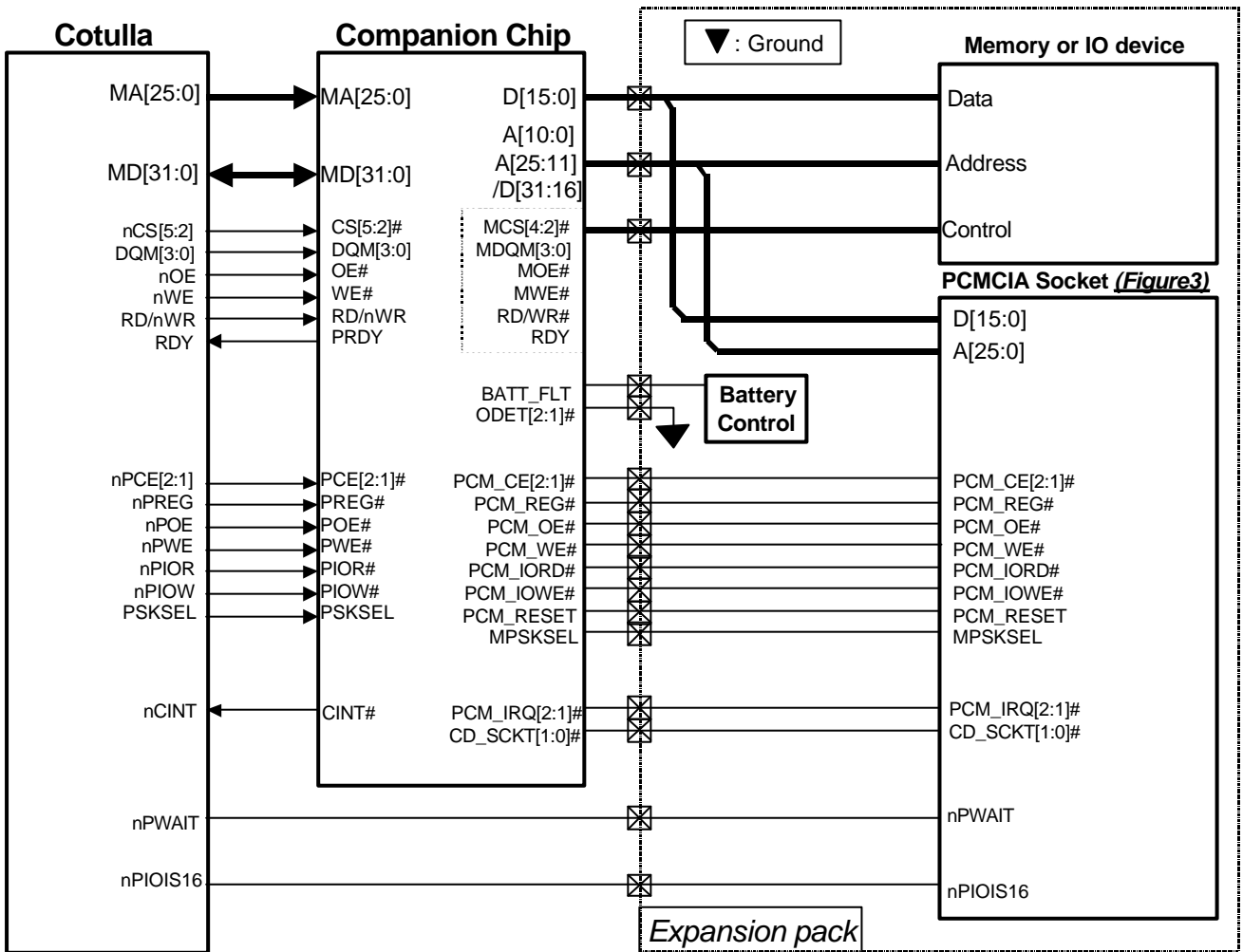
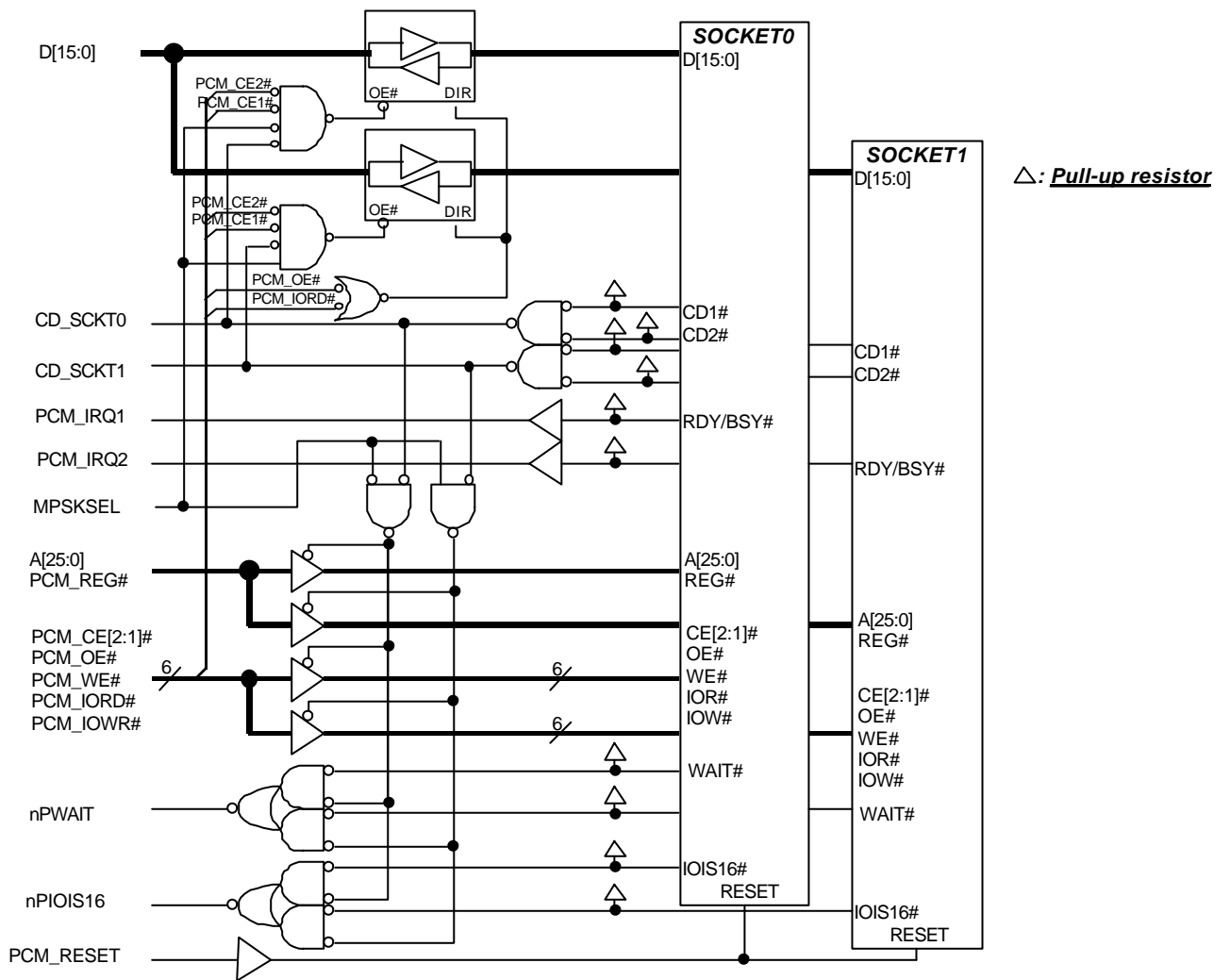


FIGURE 3. EXPANSION CARD EXTERNAL LOGIC FOR A TWO-SOCKET CONFIGURATION



## PIN DESCRIPTION

Signal	Type	Description
A[10:0]	O	PCMCIA/CF/Memory address pins used to address card or expansion pack in Memory, I/O and True IDE.
A[25:11] or D[31:16] (32-bit mode)	I/O	PCMCIA or memory address pins used to access devices in the expansion pack.  Data pins for special accesses 32-bit read and write accesses in PCMCIA, CF, I/O or memory modes. These pins are shared with A25:A11.
D[15:00] (16-bit mode)	I/O	Data pins used for 16-bit accesses in standard CF/PCMCIA, memory or I/O modes
PCM_CE[2:1]#	O	PCMCIA/CF card enable for 8 or 16-bit select in memory and I/O mode. Functions as CS0# and CS1# in IDE mode. Buffered version of Cotulla PCE[2:1].
CD_SCKT[1:0]#	I	PCMCIA/CF card detect pins for devices 1 and 2. CD_SCKT0# represents logical OR of CD1# and CD2# of PCMCIA/CF pins.  These are fed to the expansion pack block enable logic.
PCM_IORD#	O	PCMCIA/CF pin used in I/O and IDE modes as read strobe. Buffered version of Cotulla PIOR#.
PCM_IOWR#	O	PCMCIA/CF pin used in I/O and IDE modes as write strobe. Buffered version of Cotulla PLOWR#.
PCM_OE#	O	PCMCIA/CF pin used as output enable strobe. Buffered version of Cotulla POE#.
PCM_IRQ[2:1]#	I	PCMCIA/CF pins used in memory mode to determine card status for transfers. Used as an interrupt signal in I/O and IDE modes. RDY/IRQ#1 is for device 1. Route into the interrupt logic block.
PCM_RESET	O	PCMCIA/CF reset pin. CPU writes value to this bit (treat as a GPO)
PCM_REG#	O	PCMCIA/CF pin used to distinguish between common and register memory in memory mode. Buffered version of Cotulla PREG#.
PCM_WE#	O	PCMCIA/CF pin used for write strobing in to CF card in memory and I/O modes. Buffered version of Cotulla PWE#.
RDY	I	Ready signal for slow expansion pack devices to insert wait states on the variable latency I/O port

RD/WR#	O	Read/Write pin for variable latency I/O port. Buffered version of Cotulla RD/nWR.
MCS[4:2]#	O	Memory bank chip select from processor to use address and data pins for high bandwidth across expansion pack. Buffered version of Cotulla CS[4:2].
MDQM[3:0]	O	Byte enables for the 32-bit data bus of the static memory and variable latency I/O port. Buffered version of Cotulla DQM[3:0].
MOE#	O	Memory bank output enable from processor to use address and data pins for high bandwidth across expansion pack. Buffered version of Cotulla OE#.
MWE#	O	Memory bank write enable from processor to use address and data pins for high bandwidth across expansion pack. Buffered version of Cotulla WE#.
MPSKTSEL	O	PCMCIA/CF Socket select pin for expansion packs with two sockets. Buffered version of Cotulla PSKTSEL.
ODET[2:1]#	I	Expansion pack detection pins. Fed into the interrupt logic.
BATT_FLT	I	Expansion Pack Battery Fault

The following Expansion Pack inputs must be 5V tolerant:

ODET[2:1]#

RDY

PCM\_IRQ[2:1]#

CD\_SCKT[1:0]#

D[15:00]

A[25:11] / D[31:16]

The Cotulla processor supports static memory access with 6 chip selects, CS[5:0], which are configured in pairs 1:0, 3:2 and 5:4. CS0 is used for on-board ROM. The access width of CS[3:2] and CS[5:4] pairs are configured by the RBW bits in the MSC1 and MSC2 registers respectively. Similar bits are required in the companion chip so system software can match the data flow through the companion chip with the access width of Cotulla.

**REGISTER: TRANSFER DATA WIDTH(TDW)**

Register	Address	R/W	Description	Reset Value
TDW	0x000D_0000	R/W	Transfer data width	0x0000_0001

Bit	Name	Type	Description
TDW0	CS23_RBW	R/W	Width of transfers selected with CS2#, CS3# 0 = 32-bit 1 = 16-bit
TDW1	CS4_RBW	R/W	Width of transfers selected with CS4# 0 = 32-bit 1 = 16-bit
TDW2	ENDIAN	R/W	Companion chip ENDIAN mode select 0 = Little ENDIAN 1 = Big ENDIAN

32-bit transfers enable D[31:16] on the A[25:11]/D[31:16] pins. This will only occur for transfers selected by one of the CS[4:2]# chip selects where the associated RBW bit is 0.

Otherwise the transfers are 8-bit or 16-bit as defined by the Cotulla PCMCIA control signals.

## REGISTER: EXPANSION PACK STATUS(EPS)

Register	Address	R/W	Description	Reset Value
EPS	0x000D_0004	R	Expansion pack status	0x0000_0000

Bit	Name	Type	Description
EPS0	CD0	R	Socket 0 Card Detect 1 = Either no card or card is not fully inserted 0 = Card is inserted
EPS1	CD1	R	Socket 1 Card Detect 1 = Either no card or card is not fully inserted 0 = Card is inserted
EPS2	PCM_IRQ1	R	Socket 0 PCM_IREQ1 is the value of RDY/IREQ# pin 0 = Card is not ready 1 = Card is ready
EPS3	PCM_IRQ2	R	Socket 1 PCM_IREQ2 is the value of RDY/IREQ# pin 0 = Card is not ready 1 = Card is ready
EPS4	ODET1	R	Expansion Pack 1 Detect 0 = Expansion pack detected 1 = Expansion pack not detected
EPS5	ODET2	R	Expansion Pack 2 Detect 0 = Expansion pack detected 1 = Expansion pack not detected
EPS6	BATT_FLT	R	Expansion Pack Battery Fault 0 = Battery okay 1 = Battery fault

**REGISTER: CARD CONTROL(CC)**

Register	Address	R/W	Description	Reset Value
CC	0x000D_0008	R/W	Card control	0x0000_0000

Bit	Name	Type	Description
CC0	Card Reset	R/W	Socket 0,1 card reset 0 = The RESET signal to the card socket is set inactive 1 = The RESET signal to the card socket is set active

**REGISTER: INTERRUPT CONFIGURATION(IC)**

Register	Address	R/W	Description	Reset Value
IC	0x000D_000C	R/W	Interrupt configuration	0x0000_0000

Bit	Name	Type	Description
IC0	Card 0 Detect Enable	R/W	Socket 0 card detect interrupt management 0 = Card detect change management interrupt disable 1 = If card detect change, a management interrupt will occur
IC1	Card 1 Detect Enable	R/W	Socket 1 card detect interrupt management 0 = Card detect change management interrupt disable 1 = If card detect change, a management interrupt will occur
IC2	IRQ1 Enable	R/W	Socket 0 card IRQ1 interrupt management 0 = Ready change management interrupt disable 1 = If ready change, a management interrupt will occur
IC3	IRQ2 Enable	R/W	Socket 1 card IRQ2 interrupt management 0 = Ready change management interrupt disable 1 = If ready change, a management interrupt will occur
IC4	Expansion Pack1 Detect Enable	R/W	Expansion pack 1 detect interrupt management 0 = Expansion pack detect change management interrupt disable 1 = If expansion pack detect change, a management interrupt will occur
IC5	Expansion Pack2 Detect Enable	R/W	Expansion pack 2 detect interrupt management 0 = Expansion pack detect change management interrupt disable 1 = If expansion pack detect change, a management interrupt will occur
IC6	Battery Fault Enable	R/W	Battery fault interrupt management 0 = Battery fault change management interrupt disable 1 = If battery fault change, a management interrupt will occur

**REGISTER: INTERRUPT MODE(IM)**

Register	Address	R/W	Description	Reset Value
IM	0x000D_0010	R/W	Interrupt mode	0x0000_25A5

Bit	Name	Type	Description
IM[1:0]	Card 0 Detect Interrupt Mode	R/W	Socket 0 card detect interrupt mode 01 = Interrupt will occur on falling edge 10 = Interrupt will occur on rising edge 11 = Interrupt will occur on both edge
IM[3:2]	Card 1 Detect Interrupt Mode	R/W	Socket 1 card detect interrupt mode 01 = Interrupt will occur on falling edge 10 = Interrupt will occur on rising edge 11 = Interrupt will occur on both edge
IM[5:4]	IRQ1 Interrupt Mode	R/W	Socket 0 IRQ1 interrupt mode 01 = Interrupt will occur on falling edge 10 = Interrupt will occur on rising edge 11 = Interrupt will occur on both edge
IM[7:6]	IRQ2 Interrupt Mode	R/W	Socket 1 IRQ2 interrupt mode 01 = Interrupt will occur on falling edge 10 = Interrupt will occur on rising edge 11 = Interrupt will occur on both edge
IM[9:8]	Expansion Pack1 Detect Interrupt Mode	R/W	Expansion pack 1 detect interrupt mode 01 = Interrupt will occur on falling edge 10 = Interrupt will occur on rising edge 11 = Interrupt will occur on both edge
IM[11:10]	Expansion Pack2 Detect Interrupt Mode	R/W	Expansion pack 2 detect interrupt mode 01 = Interrupt will occur on falling edge 10 = Interrupt will occur on rising edge 11 = Interrupt will occur on both edge
IM[13:12]	Battery Fault Interrupt Mode	R/W	Battery fault interrupt mode 01 = Interrupt will occur on falling edge 10 = Interrupt will occur on rising edge 11 = Interrupt will occur on both edge

**REGISTER: INTERRUPT PENDING(IP)**

Register	Address	R/W	Description	Reset Value
IP	0x000D_0014	R/W	Interrupt pending	0x0000_0000

Bit	Name	Type	Description
IP0	Card 0 Detect Interrupt Pending	R/W	Socket 0 card detect interrupt pending 0 = Interrupt has not been occurred 1 = Interrupt occurred
IP1	Card 1 Detect Interrupt Pending	R/W	Socket 1 card detect interrupt pending 0 = Interrupt has not been occurred 1 = Interrupt occurred
IP2	IRQ1 Interrupt Pending	R/W	Socket 0 IRQ1 interrupt pending 0 = Interrupt has not been occurred 1 = Interrupt occurred
IP3	IRQ2 Interrupt Pending	R/W	Socket 1 IRQ2 interrupt pending 0 = Interrupt has not been occurred 1 = Interrupt occurred
IP4	Expansion Pack1 Detect Interrupt Pending	R/W	Expansion pack 1 detect interrupt pending 0 = Interrupt has not been occurred 1 = Interrupt occurred
IP5	Expansion Pack2 Detect Interrupt Pending	R/W	Expansion pack 2 detect interrupt pending 0 = Interrupt has not been occurred 1 = Interrupt occurred
IP6	Battery Fault Interrupt Pending	R/W	Battery fault interrupt pending 0 = Interrupt has not been occurred 1 = Interrupt occurred

Each bit will be cleared by writing ' 1 ' on the corresponding bit.

**REGISTER: MISC**

Register	Address	R/W	Description	Reset Value
MISC	0x000D_0018	R/W	Miscellaneous	0x0000_0001

Bit	Name	Type	Description
MISC0	USB Mask	R/W	USB Host master address masking 0 = Mask disable 1 = Mask enable

## OTHERS

The following inputs are used to enable buffers between Cotulla and the Expansion Pack:

CS[4:2]#  
 CARD\_IND#  
 IO\_EN#  
 CARD\_SCKT[1:0]#  
 OPT\_ON# (alternate function of a GPIO)  
 BATT\_FLT  
 PWR\_EN

Three Enables are generated from these signals:

Enable1 = !BATT\_FLT & !OPT\_ON# & PWR\_EN

Enable2 = (!CARD\_SCKT0# | !CARD\_SCKT1#) & Enable1

Enable3 = (!CS4# | !CS3# | !CS2#) & Enable1

The Expansion Pack Signals grouped by Enable signals:

### **Enable1**

MCS[4:2]#  
 RD/WR#  
 RDY

### **Enable2**

MPSKTSEL  
 PCM\_CE[2:1]#  
 PCM\_OE#  
 PCM\_WE#  
 PCM\_REG#  
 PCM\_IORD#  
 PCM\_IOWR#

### **Enable3**

MDQM[3:0]#  
 MWE#  
 MOE#

## I/O PAD ELECTRICAL SPECIFICATION

- 3.3V/5V-tolerant I/O with ESD slot cell.
- Driving current : 12mA