3 CLOCK & POWER MANAGEMENT (Preliminary)

OVERVIEW

The clock & power management unit consists of 2 parts, clock control unit, USB clock control unit.

The Clock control logic in SAMCOP can generate the required clock signals, GCLK for the SYSTEM bus peripherals. There are one PLL in SAMCOP. The PLL is for UCLK, dedicated for USB host block(48Mhz). The clock control unit can connect/disconnect the clock to each peripheral block of SAMCOP by S/W, which will reduce the power consumption. And When UCLK clock wants disable, setting disable bit at CLKCON SFR by S/W. SLEEP mode is entered by S/W, H/W. H/W SLEEP mode signal is POWER_EN from Cotulla device.

The power consumption will be maximized when all peripherals are turned on. The user can control the operation of peripherals by S/W. For example, if a timer is not needed, the user can disconnect the clock to the timer to reduce power.

FUNCTION DESCRIPTION

CLOCK ARCHITECTURE

Figure 3-1 shows a block diagram of the clock architecture. The main clock source comes from an external pin. SAMCOP use MCLK from COTULLA for system clock. And clock control block is controlling SYSTEM clock(GCLK) by S/W. The USB clock generator consists of an oscillator block(Oscillation Amplifier) which is connected to an external crystal, and also has one PLL (Phase-Locked-Loop) which generates the high frequency clock required in USB host module, and clock control block is controlling USB clock(UCLK) by S/W.

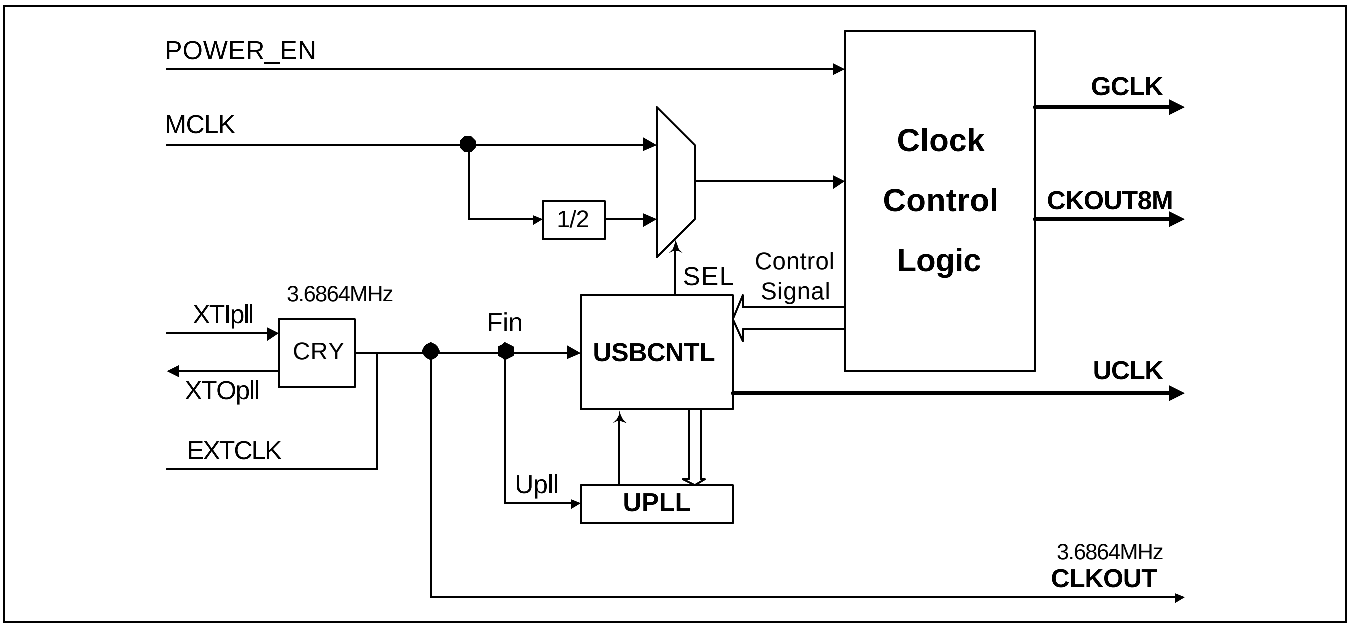

Figure 3-1. Clock Generator Block Diagram

- GCLK : System clock of SAMCOP(selectable clock)
- CKOUT8M : 8Mhz clock to External Device
- UCLK : 48Mhz USB clock (use PLL)
- CCLK : Crystal clock to COTULLA (Direct crystal clock), **3.6864Mhz**

*** USB clock selection guide**

i) Use EXTCLK -> XTIpll input clock pin must be " 1 "

ii) Use XTIpll -> EXTCLK input clock pin must be " 0 "

PLL (PHASE-LOCKED-LOOP)

The UPLL within the clock generator is the circuit which synchronizes an output signal with a reference input signal in frequency and phase. In this application, it includes the following basic blocks (Figure 3-2 shows the clock generator block diagram); the VCO(Voltage Controlled Oscillator) to generate the output frequency proportional to input DC voltage, the divider P to divide the input frequency(Fin) by p, the divider M to divide the VCO output frequency by m which is input to PFD(Phase Frequency Detector), the divider S to divide the VCO output frequency by s which is Upll(the output frequency from UPLL block), the phase difference detector, charge pump, and loop filter. The output clock frequency Upll is related to the reference input clock frequency Fin by the following equation:

$$Upll = (m * Fin) / (p * 2^{s})$$

m = M (the value for divider M)+ 8, p = P(the value for divider P) + 2

The following sections describe the operation of the PLL, that includes the phase difference detector, charge pump, VCO (Voltage controlled oscillator), and loop filter.

Phase Difference Detector(PFD)

The PFD monitors the phase difference between the Fref (the reference frequency as shown in Fig. 6-2) and Fvco, and generates a control signal(tracking signal) when it detects a difference.

Charge Pump(PUMP)

The charge pump converts the PFD control signal into a proportional charge in voltage across the external filter that drives the VCO.

Loop Filter

The control signal that the PFD generates for the charge pump, may generate large excursions(ripples) each time the Fvco is compared to the Fref. To avoid overloading the VCO, a low pass filter samples and filters the high-frequency components out of the control signal. The filter is typically a single-pole RC filter consisting of a resistor and capacitor.

Voltage Controlled Oscillator (VCO)

The output voltage from the loop filter drives the VCO, causing its oscillation frequency to increase or decrease linearly as a function of variations in average voltage. When the Fvco matches Fref in terms of frequency as well as phase, the PFD stops sending a control signal to the charge pump, which in turn stabilizes the input voltage to the loop filter. The VCO frequency then remains constant, and the PLL remains locked onto the system clock.

Usual Conditions for PLL & Clock Generator

The following conditions are generally used.

Loop filter capacitance	5 pF
External X-tal frequency	3 ~ 10 Mhz *
External capacitance used for X-tal	15 ~ 22 pF

* Value could be changed.

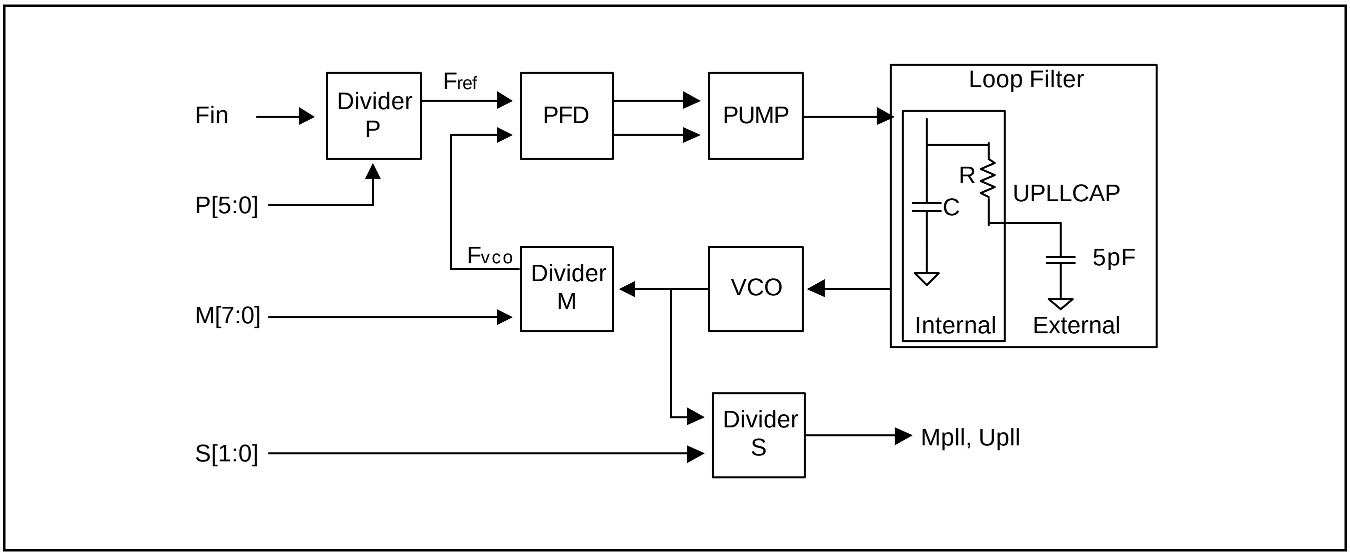

Figure 3-2. PLL (Phase-Locked Loop) Block Diagram

CLOCK CONTROL LOGIC

The clock control logic determines the clock source to be used, i.e., the direct external clock (MCLK). CLOCK CONTROL LOGIC is controlling logic disable GCLK by CLKCON SFR register. And SLEEP mode enter S/W or H/W (POWER_EN).

*** MCLK : GCLK = 1 : 2 (default)**

1. CLOCK SELECTION (Each Module)

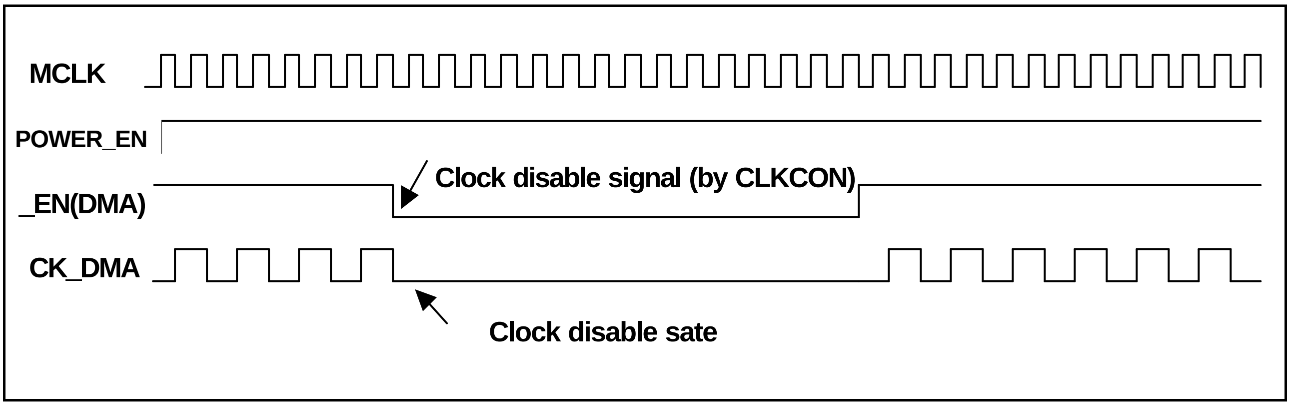

Figure 3-3. Clock Selection for DMA clock gating

2. SLEEP & WAKE_UP (software → wake-up signal)

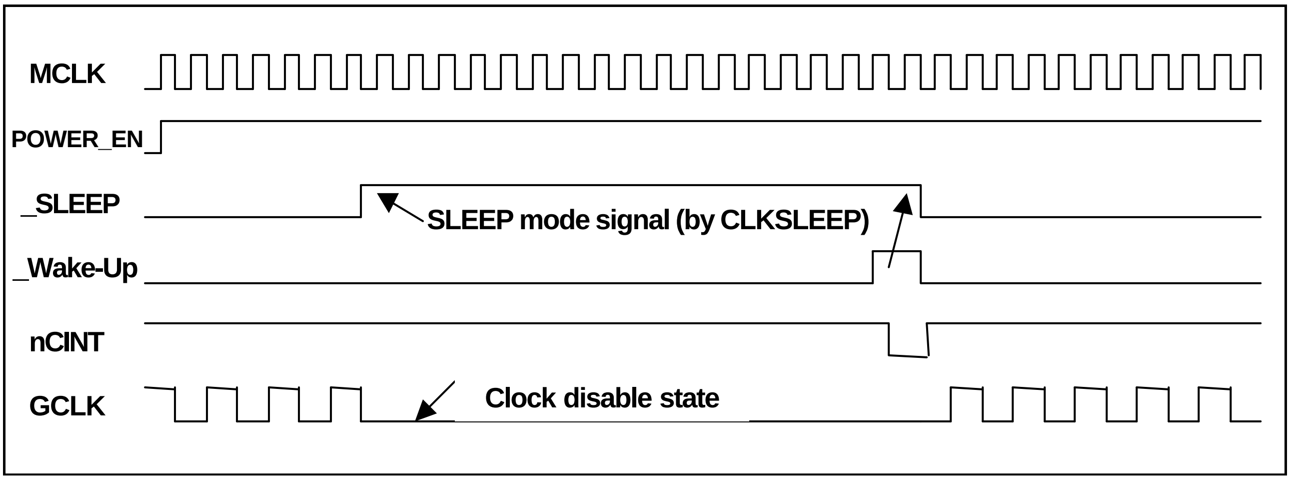

Figure 3-4. SLEEP & WAKE_UP (software → wake-up signal)

- When Wake-Up signal is generated, SLEEP mode signal of CLKSLEEP register is disable.
- Wake-Up signal → AppButton1, AppButton2, AppButton3, AppButton4, WAKEUP1, WAKEUP2, WAKEUP3, Record, SD_WAKEUP.

3. SLEEP & WAKE_UP (POWER_EN → POWER_EN)

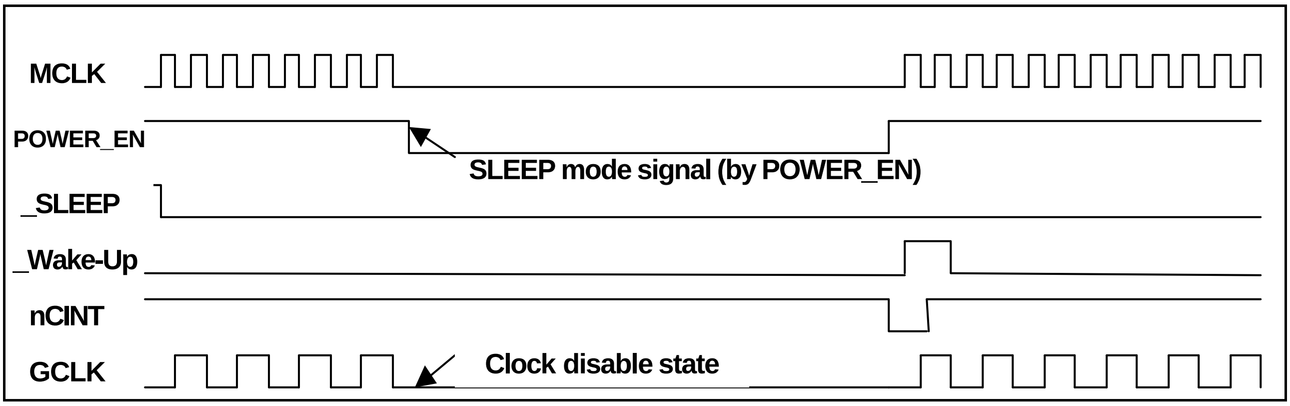

Figure 3-5. SLEEP & WAKE_UP (POWER_EN → POWER_EN)

4. SLEEP & WAKE_UP (software → POWER_EN → POWER_EN)

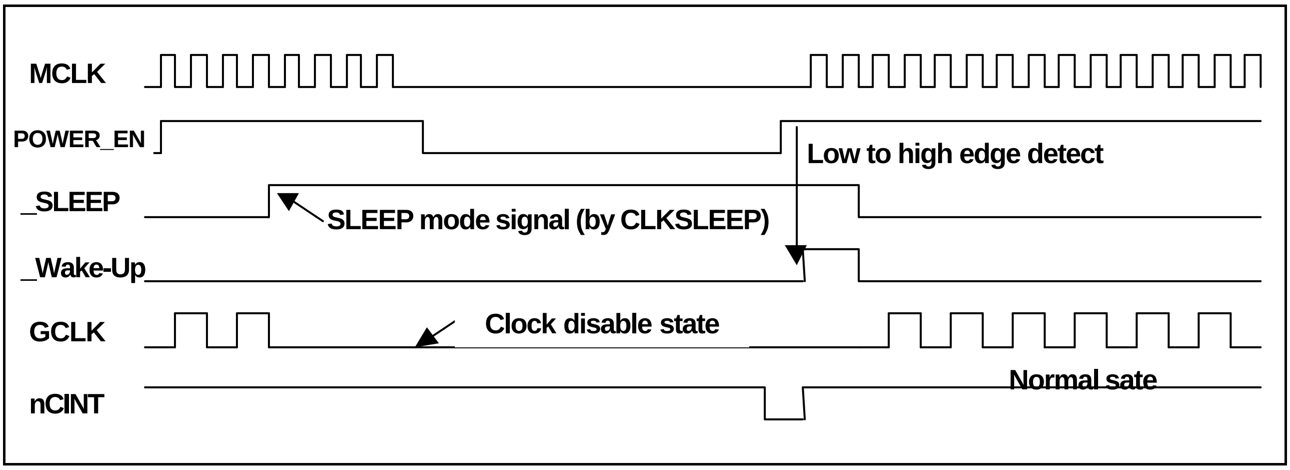

Figure 3-6. SLEEP & WAKE_UP (software → POWER_EN → POWER_EN)

- When Wake-Up signal is generated, SLEEP mode signal of CLKSLEEP register is disable.
- Wake-Up signal → As SLEEP mode enable, POWER_EN signal LOW to HIGH edge detector.
- A4_INTMSK bit should be released, and then wake-up & nCINT signal can be transferred.

USB CLOCK CONTROL LOGIC

The USB clock control logic determines the clock source to be used, i.e., the PLL clock or the direct external clock(XTIpll). When PLL is configured to a new frequency value, the USB clock control logic disables the XTIpll until the PLL output is stabilized using the PLL locking time. The USB clock control logic is also activated at power-on reset .

1. PLL Lock Time

The lock time is the minimum time required for PLL output stabilization. The lock time should be a minimum of 150us. After reset, the lock-time is inserted automatically by the internal logic with lock time count register. The automatically inserted lock time is calculated as follows;

t_lock(the PLL lock time by H/W logic) = (1/ Fin) x n, (n = U_LTIME value)

2. Power-On Reset (XTI)

Figure 3-7shows the clock behavior during the power-on reset sequence. The crystal oscillator begins oscillation within several milliseconds. When nRESET is released after the stabilization of OSC (XTIpll) clock, the PLL starts to operate according to the default PLL configuration. However PLL is commonly known to be unstable after power-on reset, so Fin fed directly to UCLK instead of the Upll(PLL output) before the S/W newly configures the UPLLCON. Even if the user wants to use the default value of UPLLCON register after reset, user should write the same value into UPLLCON register by S/W.

The PLL begins the lockup sequence again toward the new frequency only after the S/W configures the PLL with a new frequency. UCLK can be configured to be PLL output (Upll) immediately after lock time.

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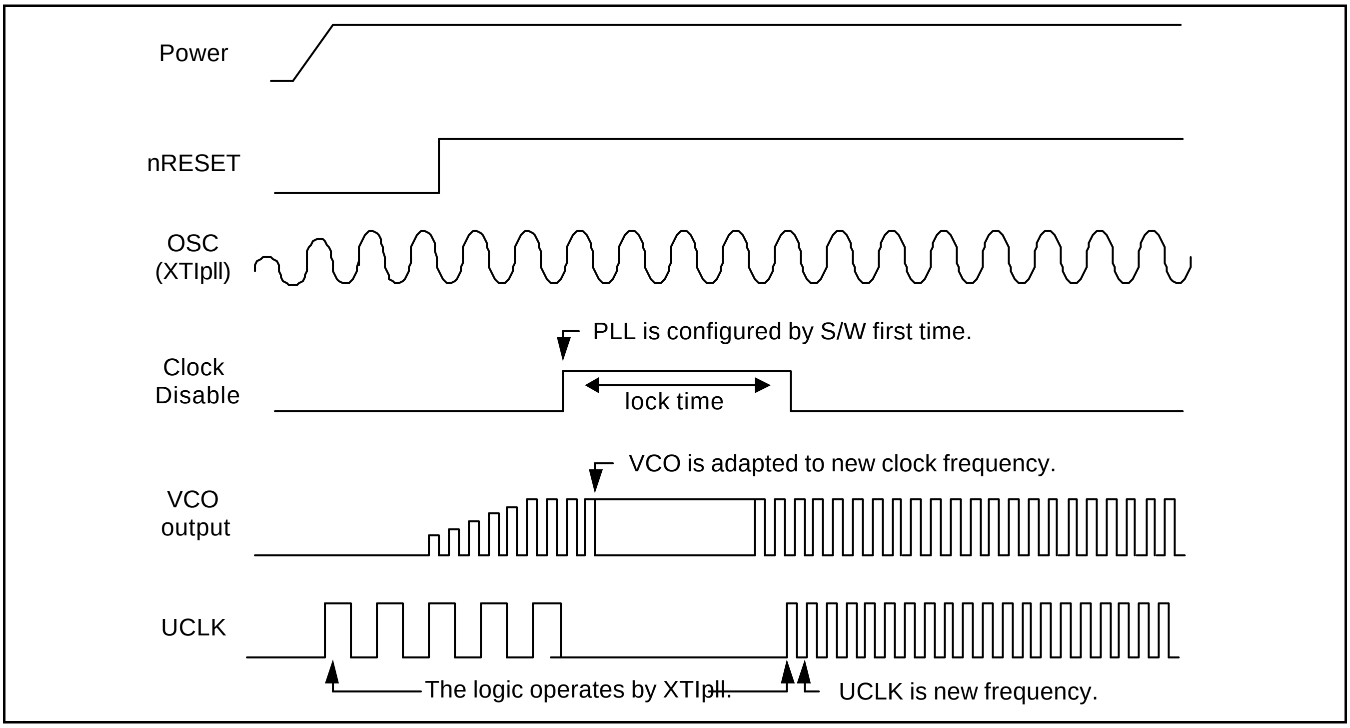

Figure 3-7. Power-On Reset Sequence

3. USB Clock Control

USB Host interface needs 48Mhz clock. In SAMCOP, The USB dedicated PLL (UPLLCON) generates 48Mhz for USB. UCLK doesn't fed until the PLL(UPLLCON) is configured.

Condition	**UCLK state**	**UPLL state**
After reset	XTI_{PLL}	on
After configuring UPLLCON, during PLL lock time	LOW state	on
After PLL lock time	48 MHz	on

POWER MANAGEMENT

The power management module controls the system clocks by software for the reduction of power consumption in SAMCOP. These schemes are related to clock control logic (GCLK). The Figure 3-8depicts the clock distribution of SAMCOP.

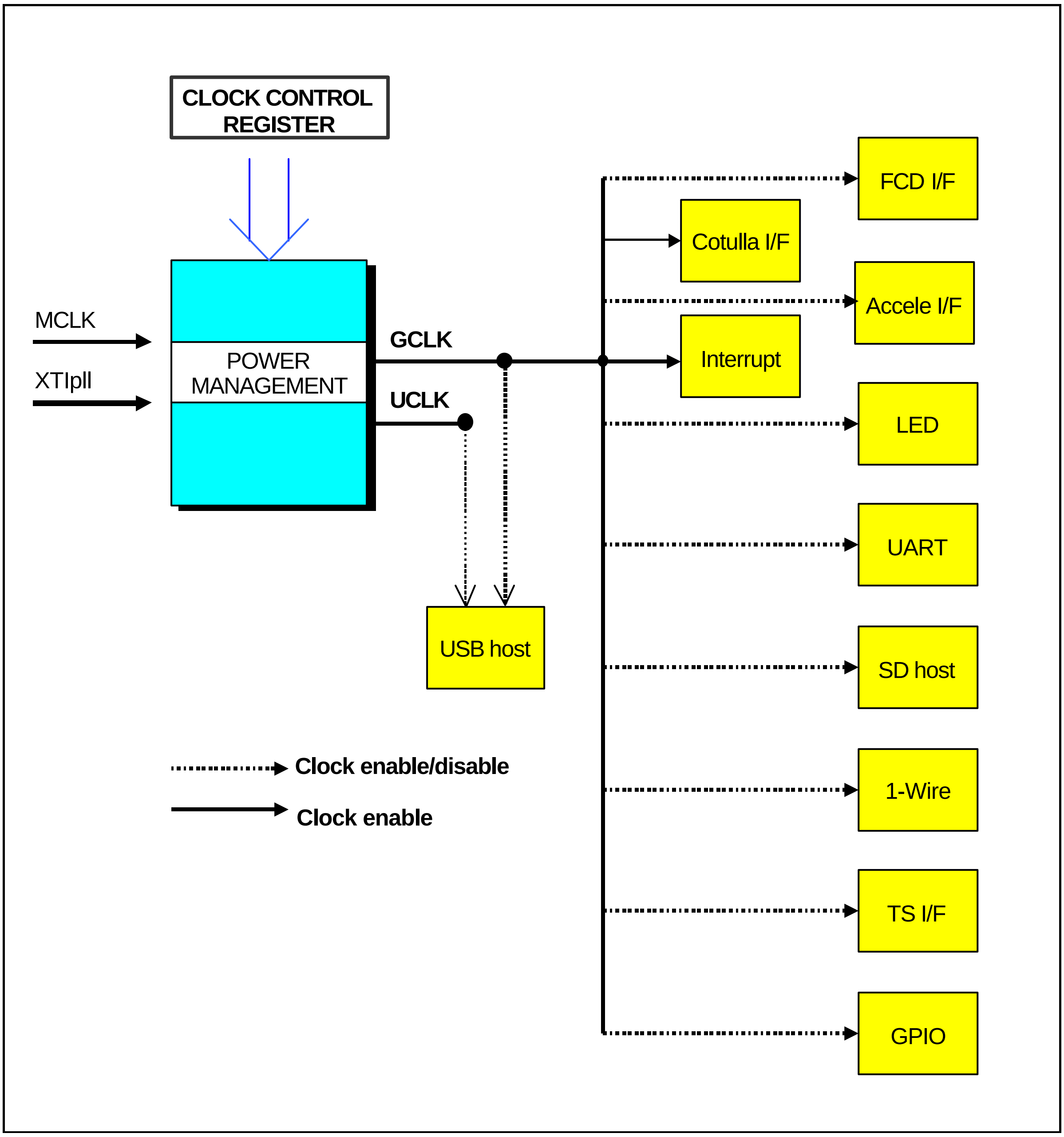

Figure 3-7 the Clock Distribution Block Diagram

CLOCK GENERATOR & POWER MANAGEMENT SPECIAL REGISTER

LOCK TIME COUNT REGISTER (LOCKTIME)

Register	Address	R/W	Description	Reset Value
LOCKTIME	0x0005_0000	R/W	PLL lock time count register	0x00000fff

LOCKTIME	Bit	Description	Initial State
U_LTIME	[11:0]	UPLL lock time count value for UCLK. (U_LTIME>150uS)	0xfff

PLL CONTROL REGISTER (UPLLCON)

$$Upll = (m * Fin) / (p * 2^s)$$
$$m = (MDIV + 8),\ \ p = (PDIV + 2),\ \ s = SDIV$$

P, M, S selection guide

UPLLCON value(P, M, S) must be confirmed by SAMSUNG.

Register	Address	R/W	Description	Reset Value
UPLLCON	0x0005_0004	R/W	UPLL configuration register	0x00028080

PLLCON	Bit	Description	Initial State
MDIV	[19:12]	Main divider control	0x28
PDIV	[9:4]	Pre-divider control	0x08
SDIV	[1:0]	Post divider control	0x0

CLOCK CONTROL REGISTER (CLKCON)

Register	Address	R/W	Description	Reset Value
CLKCON	0x0005_0008	R/W	Clock generator control Register	0x00000ffe

CLKCON	Bit	Description	Initial State
1-Wire Bus Master	[11]	Controls GCLK into 1-Wire bus master block 0 = Disable, 1 = Enable	1
Accelerometer I/F	[10]	Controls GCLK into accelerometer interface block 0 = Disable, 1 = Enable	1
LED	[9]	Controls GCLK into LED driver block. 0 = Disable, 1 = Enable	1
UART1	[8]	Controls GCLK into UART1 block 0 = Disable, 1 = Enable	1
UART0	[7]	Controls GCLK into UART0 block 0 = Disable, 1 = Enable	1
Touch Panel I/F	[6]	Controls GCLK into Touch Panel interface block 0 = Disable, 1 = Enable	1
SD host	[5]	Controls GCLK into SD host block 0 = Disable, 1 = Enable	1
FCD I/F	[4]	Controls GCLK into FCD interface block 0 = Disable, 1 = Enable	1
GPIO	[3]	Controls GCLK into GPIO block 0 = Disable, 1 = Enable	1
DMA	[2]	Controls GCLK into DMA block 0 = Disable, 1 = Enable	1
USB host	[1]	Controls GCLK into USB host block 0 = Disable, 1 = Enable	1
UCLK_ON	[0]	0: UCLK ON (UPLL is also turned on and the UPLL lock time is inserted automatically.) 1: UCLK OFF(UPLL is also turned off)	0

CLKSLEEP CONTROL REGISTER (CLKSLEEP)

Register	Address	R/W	Description	Reset Value
CLKSLEEP	0x0005_000c	R/W	CLOCK SLEEP control register	0x00000000

CLKSLOW	Bit	Description	Initial State
UCLK_ON	[2]	0 : normal state 1 : when SAMCOOP enter sleep mode by PWR_EN, UCLK(UPLL) is automatically off.	0
HALF_CLK	[1]	0 : main clock (GCLK) is 1/2 MCLK 1 : main clock (GCLK) is MCLK	0
SLEEP	[0]	0 : normal mode(all clock is controlling by CLKCON) 1 : S/W sleep mode(all clock disable) The wake-up is done by only the wake-up signal of SAMCOP. This bit is automatically cleared to 0 at the wake-up.	0