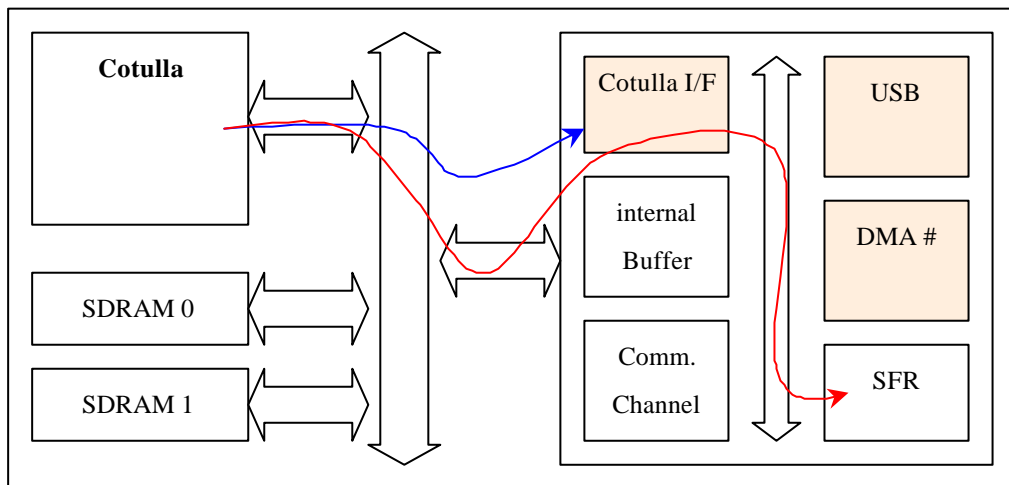


2 COTULLA INTERFACE & 32KB Internal SRAM (Pre.)

DATA TRANSFER PROTOCOL BETWEEN SAMCOP AND MCU

1. Variable Latency I/O transfer through MCU Memory Map

- 1) SFR Read/Write Cycle to Control Some Hardware Through the SAMCOP
 - i. This mode is frequently used when MCU read or writes the SFR (Special Function Registers) within SAMCOP.
 - ii. MCU can access the SAMCOP' s SFR in native way.
 - iii. Cotulla Interface module executes this cycle as a master of AMBA AHB.



The address from Cotulla is determined by the hardware chip select signal and it has affixed memory bank. (for example, if nCS2 of SAMCOP connected to nCS, the base address becomes 0x08000000).

ARCHITECTURE OF SAMCOP

1. Master/Slave Modules

A. Masters :

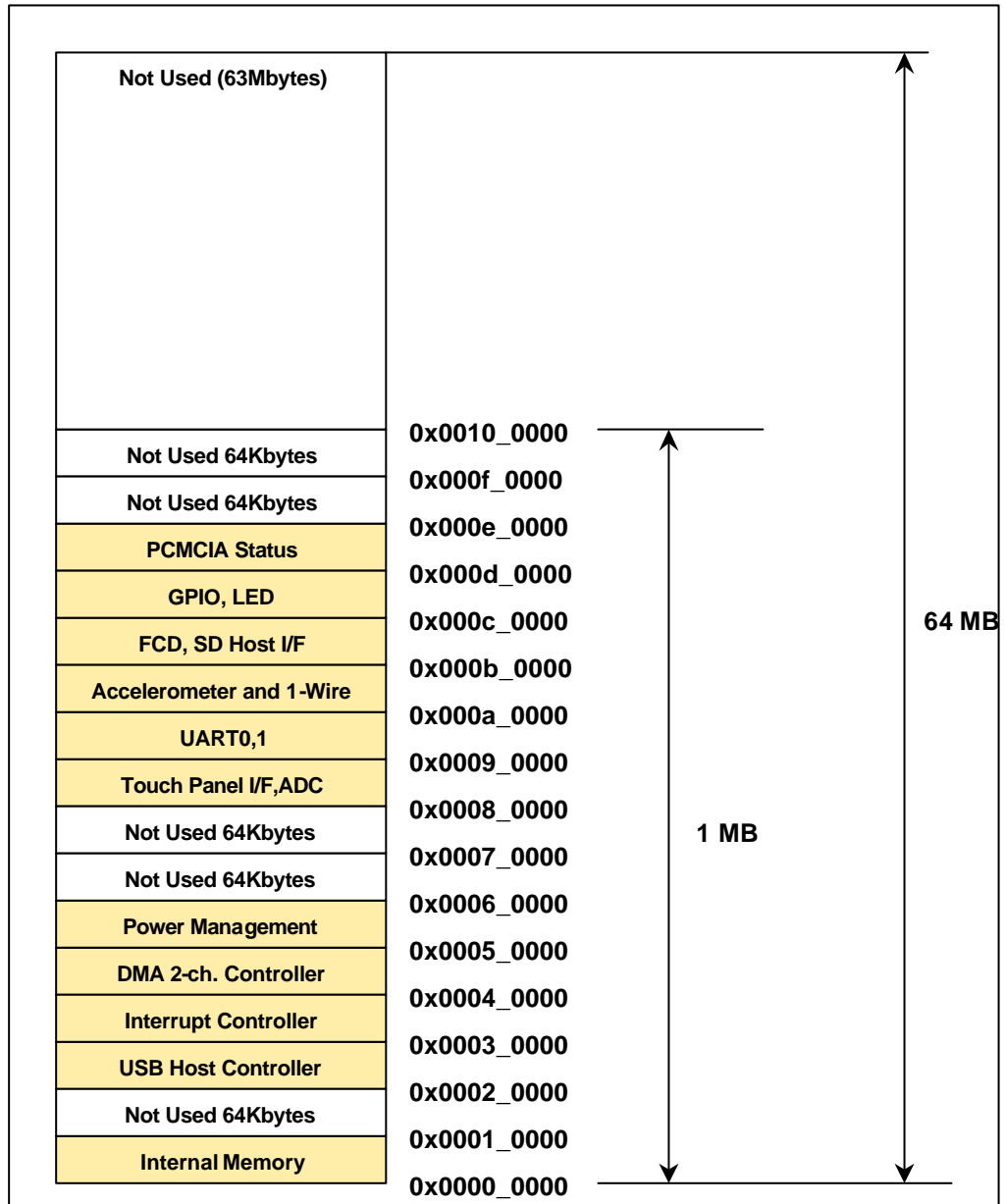
- i. Cotulla I/F : Control data transfer from MCU to SFR (using AHB Single mode)
- ii. DMA0 to 1 : DMA is started by software, peripheral modules or external pins. (using AHB incremental 4 burst mode)
- iii. USB Host : USB Transmission, Receive : AHB Single (Write for Byte, Read for Word size)

B. Slaves :

- i. Internal Buffer 32 Kbytes : Internal SRAM Buffer(0x0~0x7fff).
- ii. SFR(Special Function Register Files of AHB, and APB)

2. Memory Map

A. The Memory Map on the SAMCOP side

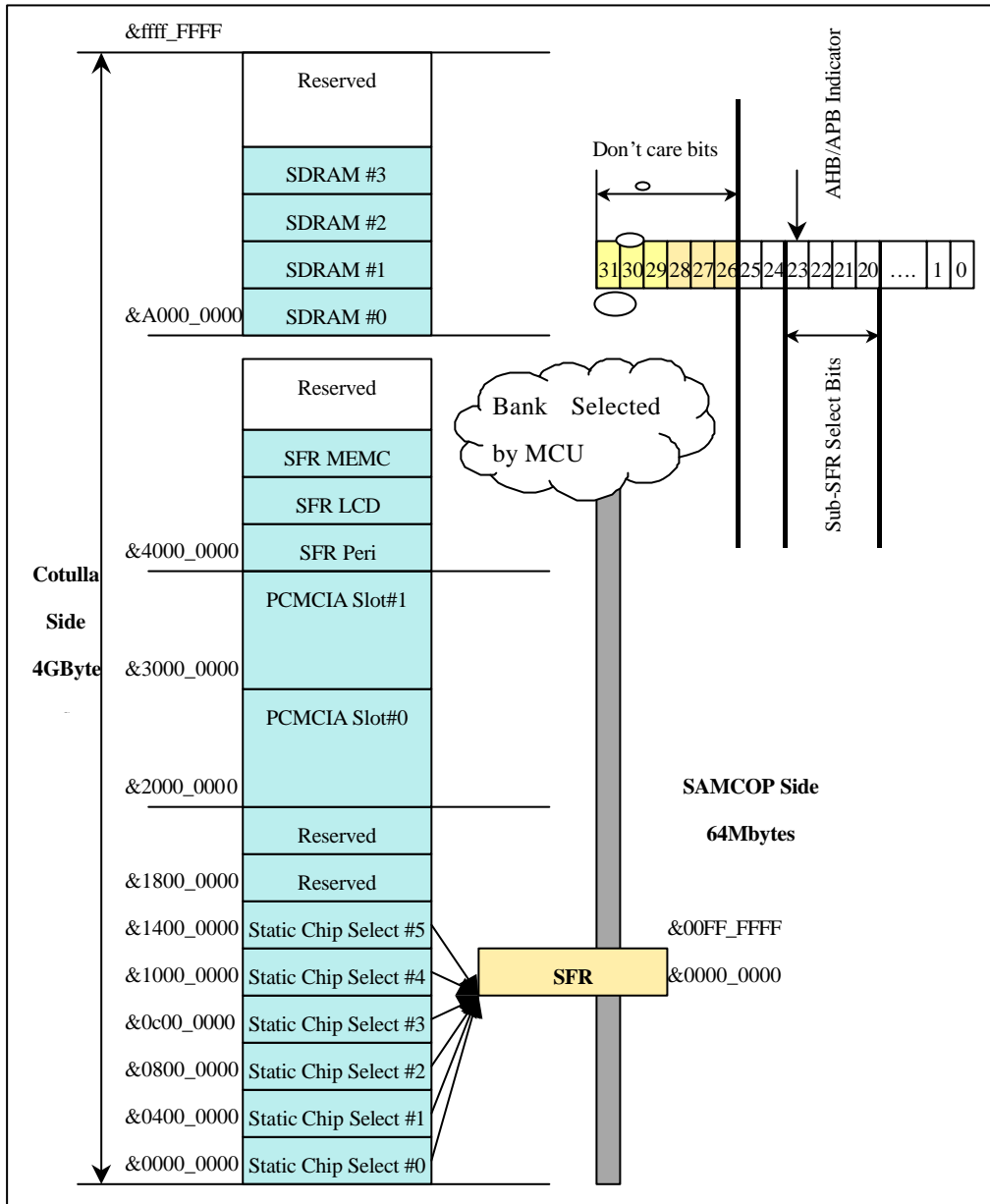


SAMCOP uses internally the valid address 25bits

The 32KB internal memory(SRAM) area is 0x00000000~0x00007fff.



B. The Memory Map on the MCU side



C. PCMCIA is just extension of slot and there is no memory space allocated from SAMCOP.

D. Special Function Register List

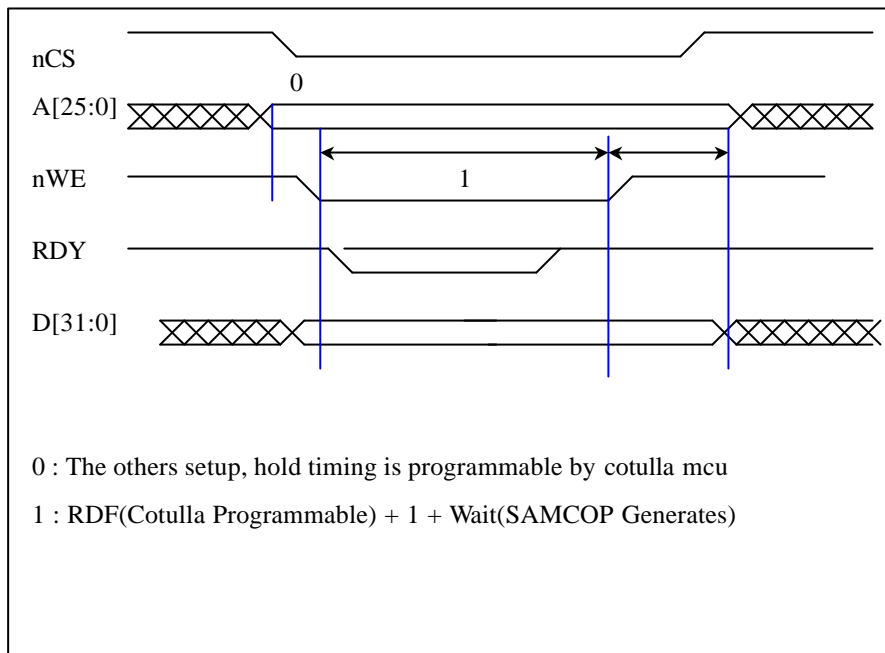
SFR' s address is determined by the static chip select signal 1thru 5.

(See Appendix I)

3. Timing Diagram

A. Variable Latency IO Mode

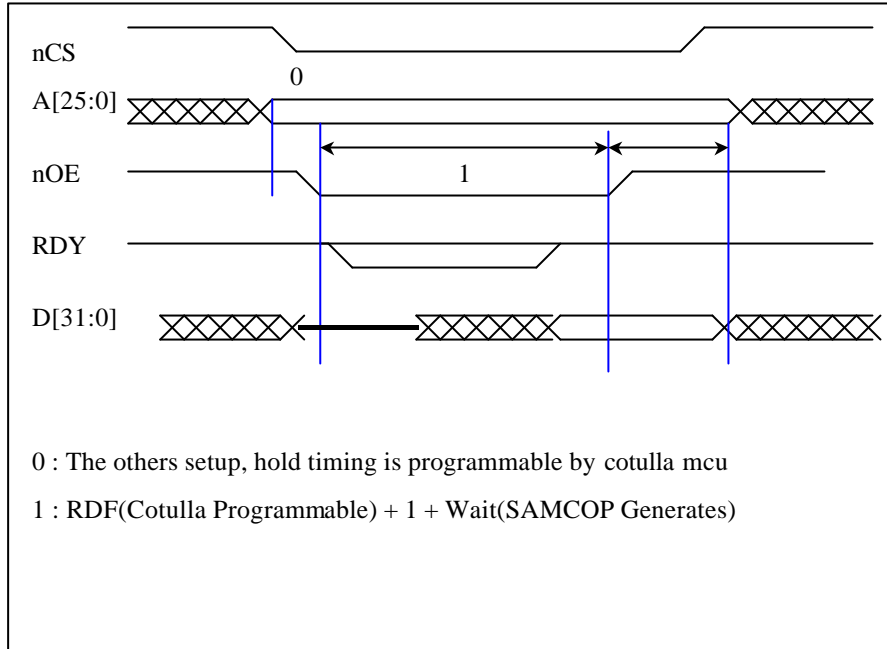
i. SFR Write Cycle with Variable Latency



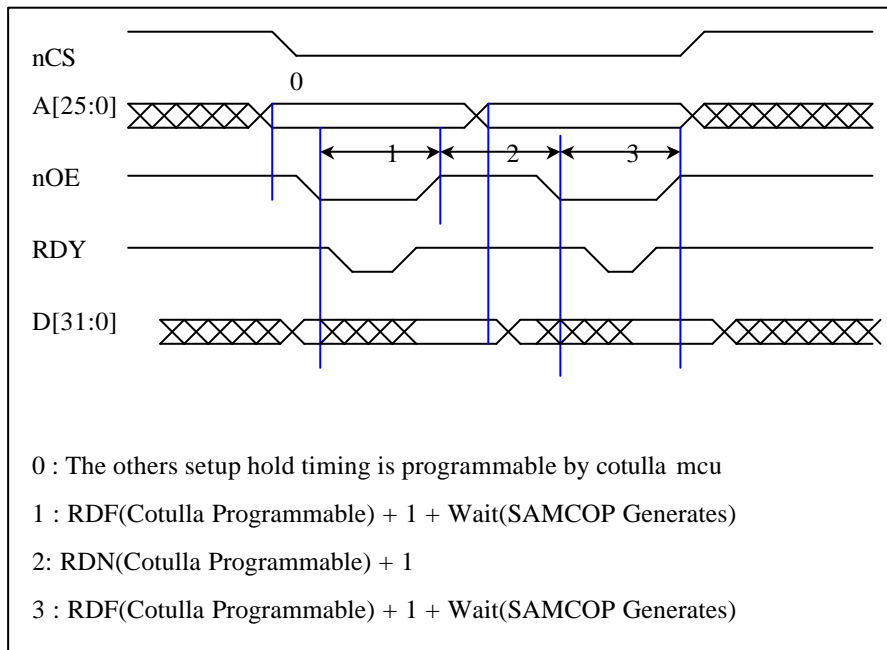
Basically this timing is similar to the Asynchronous SRAM Timing. RDY is used to signal MCU to wait until SAMCOP transfer DATA to BUS from SFR



ii. SFR Read Cycle with Variable Latency

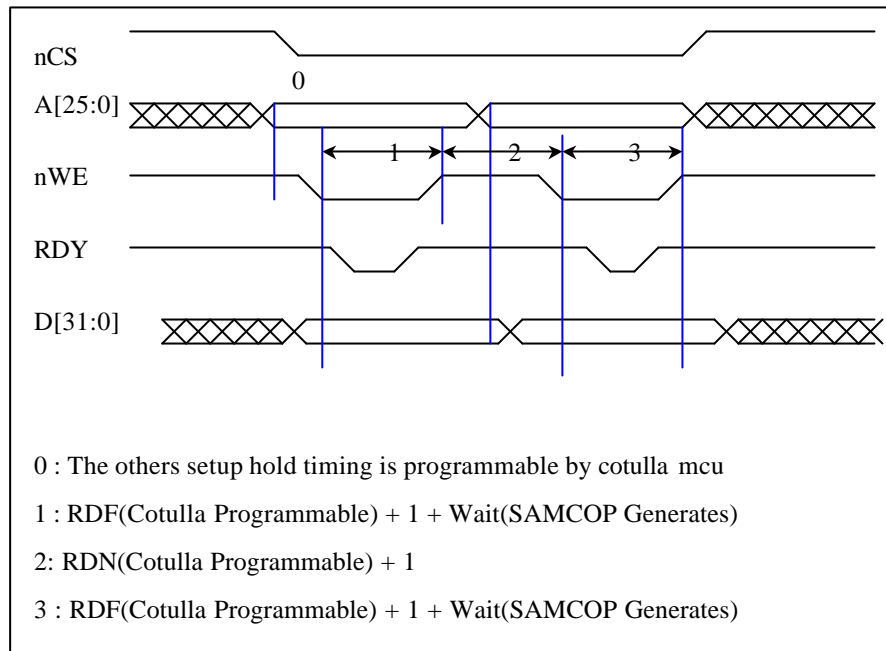


iii. SFR Read Burst Cycle with Variable Latency



The timing is determined by RDF and RDN which is programmable from MCU. However, SAMCOP is operated in single cycle..

iv. SFR Write Burst Cycle with Variable Latency



B. Cotulla Flow through DMA Mode

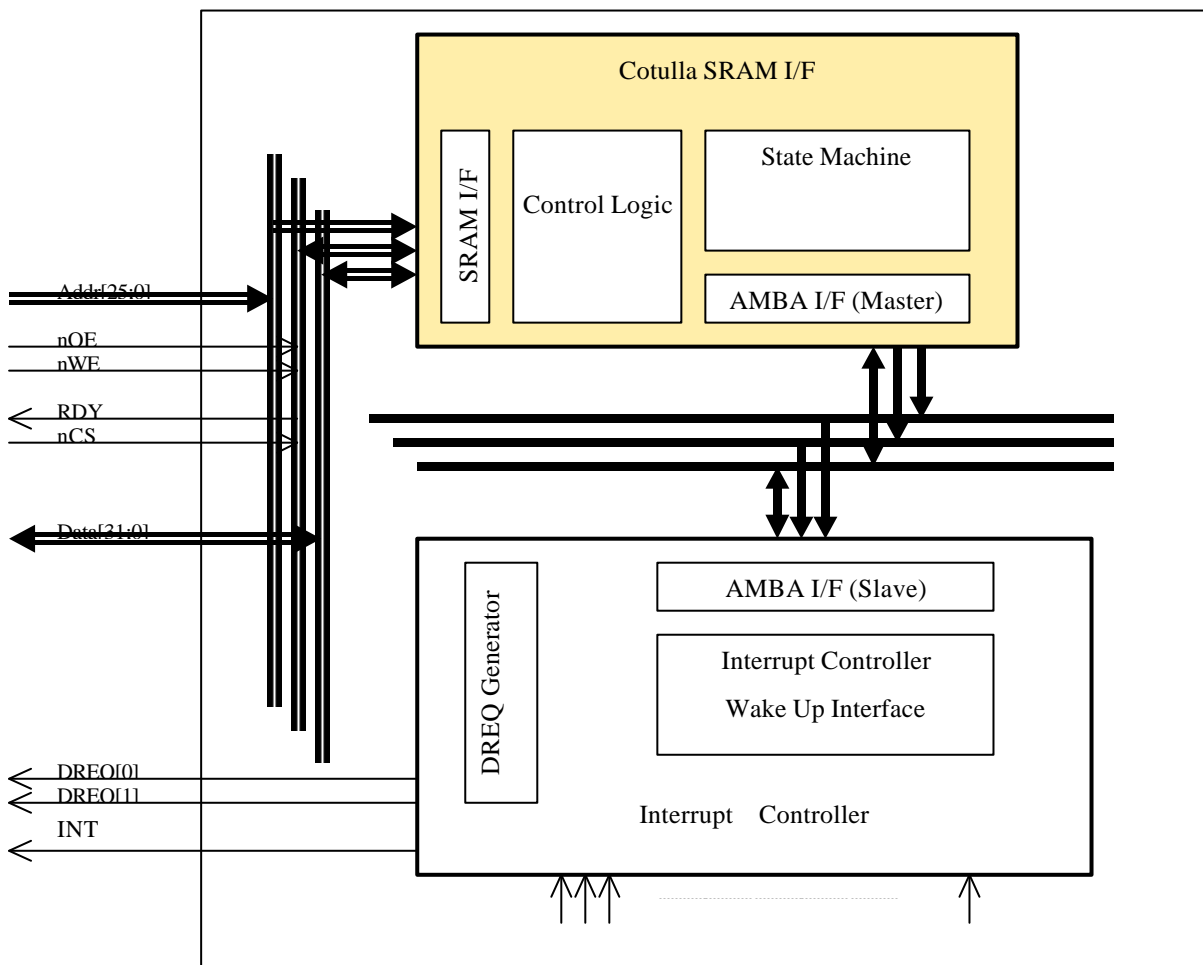
- i. It is same to Latency IO Read Write Timing

DESIGN CONSIDERATION

1. Cotulla Interface

A. Cotulla SRAM Bank Interface

This is Variable Latency IO Mode from Cotulla. In this mode, the module is slave to MCU via SRAM Interface and RDY Signal Control Slave Operation. To the SAMCOP it is master of AMBA AHB. Though MCU works in burst mode, It will be operate only the single transfer mode of AMBA AHB.



The external DMA mode which is supported by cotulla is the flow through mode.

2. Internal Buffer

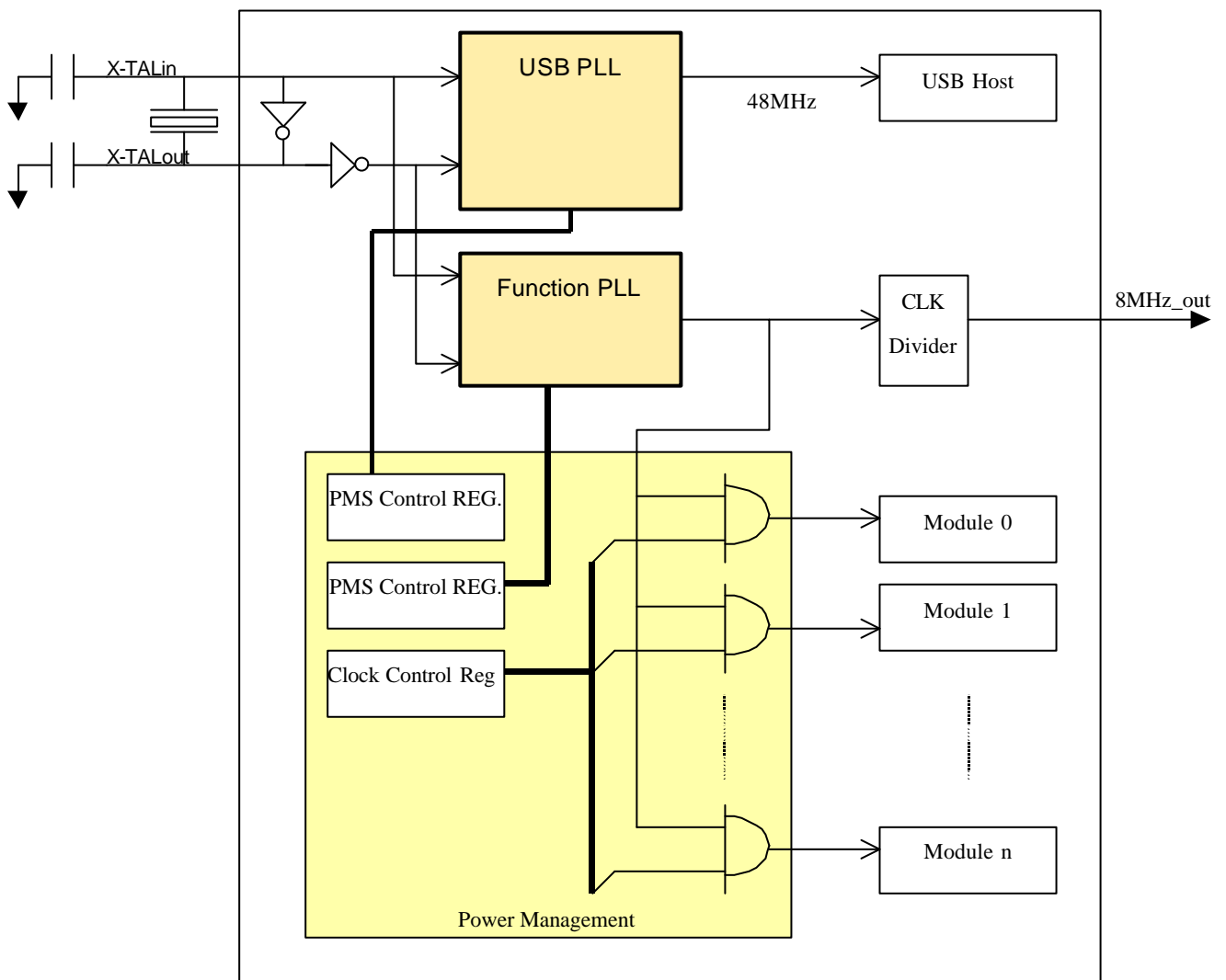
This buffer is a slave module of AMBA AHB, which can be accessed from Cotulla I/F.

3. Clock Control Scheme

A. Module Stop Mode

Clocks to all modules in SAMCOP can be controlled by Power Management Block. Software can disable by writing 0 to the respective control bit.

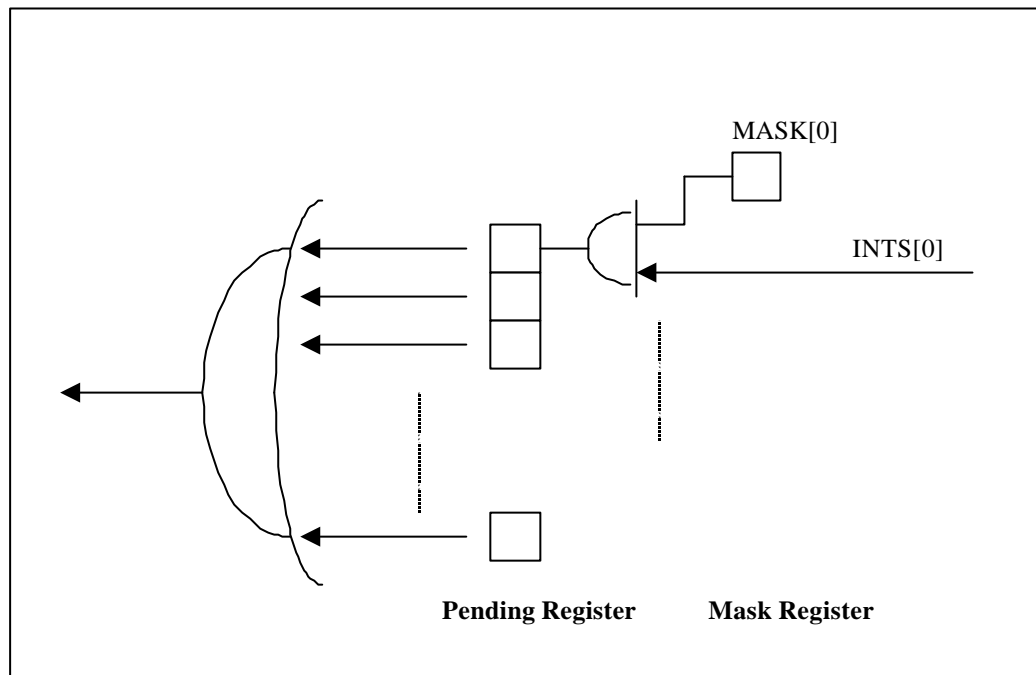
B. function PLL and USB Dedicated PLL



4. Interrupt and Wakeup

A. Interrupt

Interrupt informs Cotulla from any interrupt source within SAMCOP. It provides pending and masking service for each interrupt source as shown in the figure.



B. Wakeup

- i. Wakeup signal will be generated from combinational logic independent from any clocking source..

ii. Concept of Wakeup function in Interrupt Controller

