

# 6 NAND FLASH CONTROLLER

## OVERVIEW

Recently, the NOR flash memory is expensive but SDRAM and NAND flash memory are inexpensive, some users want to execute boot code on NAND flash and execute the main code on SDRAM.

HAMCOP boot code can be executed on external NAND flash memory. In order to support NAND flash boot loader, there is an internal SRAM(16-KB) buffer. This internal SRAM buffer is called 'Steppingstone'. When booting, the 16-KB of the NAND flash memory will be loaded into Steppingstone and boot code loaded into Steppingstone will be executed.

## FEATURES

- 1) NAND Flash mode: A user can read/erase/program NAND flash memory by S/W.
- 2) Auto boot mode: Boot code is transferred into Steppingstone(16KB SRAM) during reset duration. After transfer, Boot code will be executed on the Steppingstone(Supports only little endian mode).
- 3) Support 256(or 512) Bytes/page NAND Flash memory.
- 4) Support 3(or 4) Address cycles NAND Flash memory.
- 5) Support 8(or 16) bits memory I/F bus.
- 6) Hardware ECC detecting block(H/W detecting and S/W correcting)
- 7) 26 bits address area(support up to 64MBytes).
- 8) SFR I/F: Half word(only Little Endian).
- 9) Stepping Stone I/F: Half word
- 10) The Steppingstone 16-KB internal SRAM buffer can be used for another purpose after NAND flash booting.

BLOCK DIAGRAM

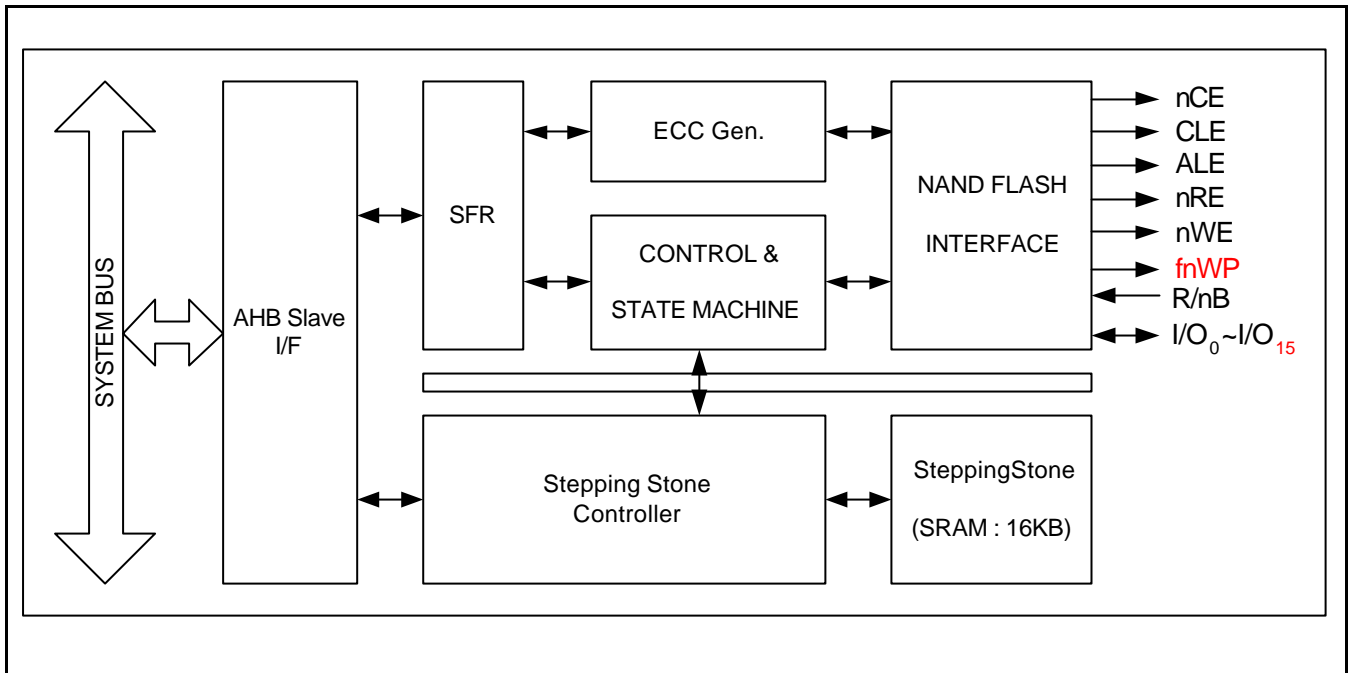


Figure 6-1. NAND Flash Controller Block Diagram

OPERATION SCHEME

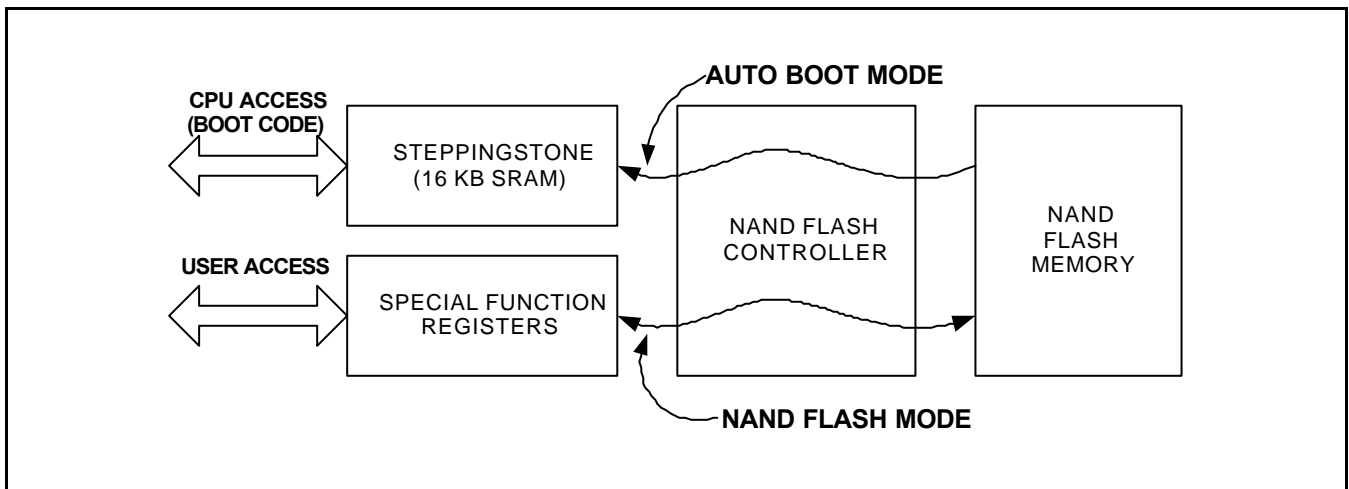


Figure 6-2. NAND Flash Operation Scheme

**AUTO BOOT MODE SEQUENCE**

- 1) After reset.
- 2) If the auto boot mode is enabled, the first 16-KB of NAND flash memory is copied onto Steppingstone 16-KB internal buffer.
- 3) CPU starts to execute the boot code on the Steppingstone 16-KB internal buffer.

**NOTE:** During the auto boot mode, the ECC is not checked. So, The first 16-KB of NAND flash should have no bit error.

**NAND FLASH MODE**

- 1) Configure NAND flash configuration by NFCONF register.
- 2) Write NAND flash command onto NFCMD register.
- 3) Write NAND flash address onto NFADDR register.
- 4) Read/Write data while checking NAND flash status by NFSTAT register. R/nB signal should be checked before read operation or after program operation.

**NAND FLASH MEMORY TIMING**

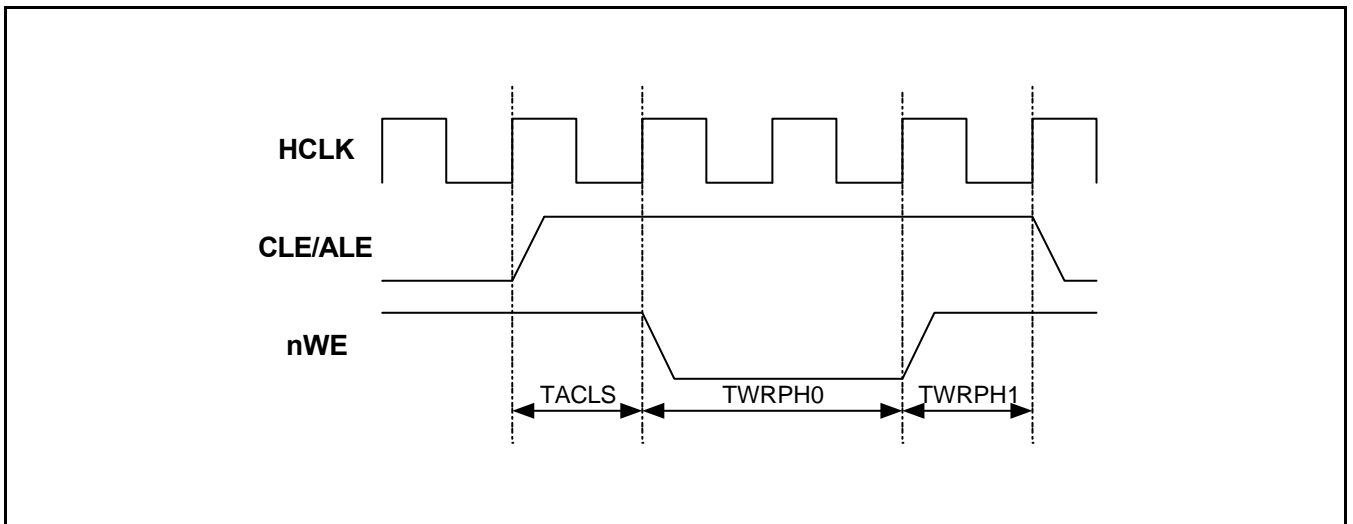


Figure 6-3. TACLS=1, TWRPH0=1, TWRPH1=0

## Function Description

Address and Data bus as one memory Port in HAMCOP are assigned by 26bits and 16bits in each. 8/16-bit data can be transferred and Max 64MB Memory can be attached.

When Booting, 8bits or 16 bit I/F should be decided by the "fWidthSel" signal status. If fWidthSel bit is 0, then Boot code will be loaded by NAND Flash memory, which is set as fIO[7:0], and if fWidthSel bit is 1, Boot code will be loaded by NAND Flash memory, which is set as fIO[15:0].

## Boot Loader Function

If a Chip is reset such as System Power-On, etc, Boot code of NAND Flash Memory(BANK0, Start Address is 0x0) is loaded to the Stepping stone automatically. While booting, other masters such as CPU(ARM Core) and etc, should be halted until NAND Boot loading is completed.

The size of the first Block of NAND flash should be 16KBytes. Because the first block of NAND Flash Memory must be guaranteed as "no invalid block" by the Provider. If the first block size is 8KBytes or the first block has invalid bit, then Boot loading can be failed.

To do Boot loading rightly, the below 4 signals should be set before the Reset.

- **fWidthSel** : This signal is used to notify NAND Flash Memory Bus Width to NAND Flash controller. When Booting, Boot loader will load data by referring to this bit.
  
- **fPageSel** : This signal notify the Page size of NAND Flash Memory. 256(or 512) Bytes/page size is supported.
  
- **fAddrStep** : This signal notify Address Cycle of NAND Flash Memory. 3(or 4) address cycles NAND Flash memory is supported.

**NOTE** : ECC will not be executed during NAND Booting, so there should be no bit fail in the first block(16KB) of NAND Flash memory.

### NAND Flash Function

A user should control NAND Flash memory in personal if it is in need. Many functions such as Block Erase, Read Status, etc are need to access NAND Flash memory. But NAND Flash Controller does not support all functions as above, so a user should control NAND Flash memory with using NAND Flash mode.

Only [7:0]bits of Command and Address register have valid values in NAND Flash mode, and those values will be output through fIO[15:8] and fIO[7:0]. Data register[15:0] will be mapped(corresponded) to fIO[15:0] directly.

**NOTE** : SFR(Special Function Register)s of NAND Flash Controller can be accessed by Half Word, and can be supported only by Little Endian. This NOTE can be applied to all SFRs of HAMCOP.

**Stepping Stone(Internal SRAM 16KBytes)**

- Stepping Stone is 16KBytes SRAM.
- This area(Stepping Stone) can be used as an optional memory(SRAM), regardless of using NAND Flash Controller.
- Stepping Stone support Little/Big Endian modes and Half-word/Byte access.

**ECC(Error Correction Code)**

- NAND Flash Controller make ECC and provide the way to detect the fail bit of memory by Hardware. The supported ECC module is corresponded to 512Bytes. Two ECC modules are used for fIO[15:8] and fIO[7:0] each.
- These ECC modules make ECC for every Read/Write data of NAND Flash memory, so a user should reset the ECC value with page unit through InitECC bit of Control register.

**NOTE :** ECC module support for two 8-bit NAND Flash memory each. If a user use NAND Flash memory of 16-bit fIO, ECC will be occurred for [15:8] and [7:0] each and those ECC values should be stored at the spare area.

**PIN configuration**

Name	Type	Source/Destination	Description
fnCE	Output	Pad	Chip Enable
fCLE	Output	Pad	Command Latch Enable
fALE	Output	Pad	Address Latch Enable
fnRE	Output	Pad	Read Enable
fnWE	Output	Pad	Write Enable
fRnB	Input	Pad	Ready/Busy for I/O[7:0]
fIOin[15:0]	In/Out	Pad	Data Input/Output
fnWP	Output	Pad	NAND Flash Write Protection

fIO[15:0] : Data/Command/Address In/Out Port(shared with the data bus)

fIO[15:8] is muxed with GPC[7:0]

fCLE : Command Latch Enable(Output)

fALE : Address Latch Enable(Output)

fnCE : NAND Flash Chip Enable(Output)

fnRE : NAND Flash Read Enable(Output)

fnWE : NAND Flash Write Enable(Output)

fRnB : NAND Flash Ready/nBusy(Input)

fnWP : NAND Flash Write Protection (Output)

**BOOT AND NAND FLASH CONFIGURATIONS**

1) OM[2:0] = 000b : Enable NAND Flash controller auto boot mode

2) fPageSel: NAND Flash memory page size selection

0 : 256 Bytes/Page

1 : 512 Bytes/Page

3) fAddrCycles: NAND Flash memory address step selection

0 : 3 Cycles addressing

1 : 4 Cycles addressing

4) fWidthSel: NAND Flash memory IO width selection

0 : 8 bit IO

1 : 16 bit IO

**512 BYTE ECC PARITY CODE ASSIGNMENT TABLE**

	DATA7	DATA6	DATA5	DATA4	DATA3	DATA2	DATA1	DATA0
<b>ECC0</b>	P64	P64'	P32	P32'	P16	P16'	P8	P8'
<b>ECC1</b>	P1024	P1024'	P512	P512'	P256	P256'	P128	P128'
<b>ECC2</b>	P4	P4'	P2	P2'	P1	P1'	P2048	P2048'

HAMCOP generates 512 bytes ECC Parity Code during Write / Read operation. ECC Parity Code consists of 3byte per 512byte data.

$$24\text{bit ECC Parity Code} = 18\text{bit Line parity} + 6\text{bit Column Parity}$$

ECC generator block executes the followings:

- 1) When MCU writes data to NAND, ECC generator block generates ECC code.
- 2) When MCU reads data from NAND, ECC generator block generates ECC code and compare it with pre-written ECC code.

## Programmer's Model

### Configuration Register

Register	Address	R/W	Description	Reset Value
<b>NFCNF0</b>	0x5000	R/W	NAND Flash Configuration register	-

NFCNF0	Bit	Description	Initial State
<b>TACLS</b>	[14:12]	CLE & ALE duration Setting Value (0~7) Duration = HCLK * TACLS	001
Reserved	[11]	Reserved	0
TWRPH0	[10:8]	TWRPH0 duration Setting Value (0~7) Duration = HCLK * ( <b>TWRPH0</b> +1 )	000
Reserved	[7]	Reserved	0
TWRPH1	[6:4]	TWRPH1 duration Setting Value (0~7) Duration = HCLK * ( <b>TWRPH1</b> +1 )	000
<b>HW_nCE</b>	[3]	Hardware Flash_nCE control 0 : Do not supports Flash_nCE control(Manual set) 1 : Supports Flash_nCE control	0
<b>BusWidth</b>	[2]	NAND Flash Memory I/O bus width 0 : 8-bit bus <b>1 : 16-bit bus</b>	H/W Set (Read only)
PageSize	[1]	Auto Load Page Size of NAND Flash Memory 0 : 256 Bytes,                1 : 512 Bytes,	H/W Set (Read only)
AddrCycle	[0]	Address Cycle of NAND Flash Memory 0 : 3 address cycles    1 : 4 address cycles	H/W Set (Read only)

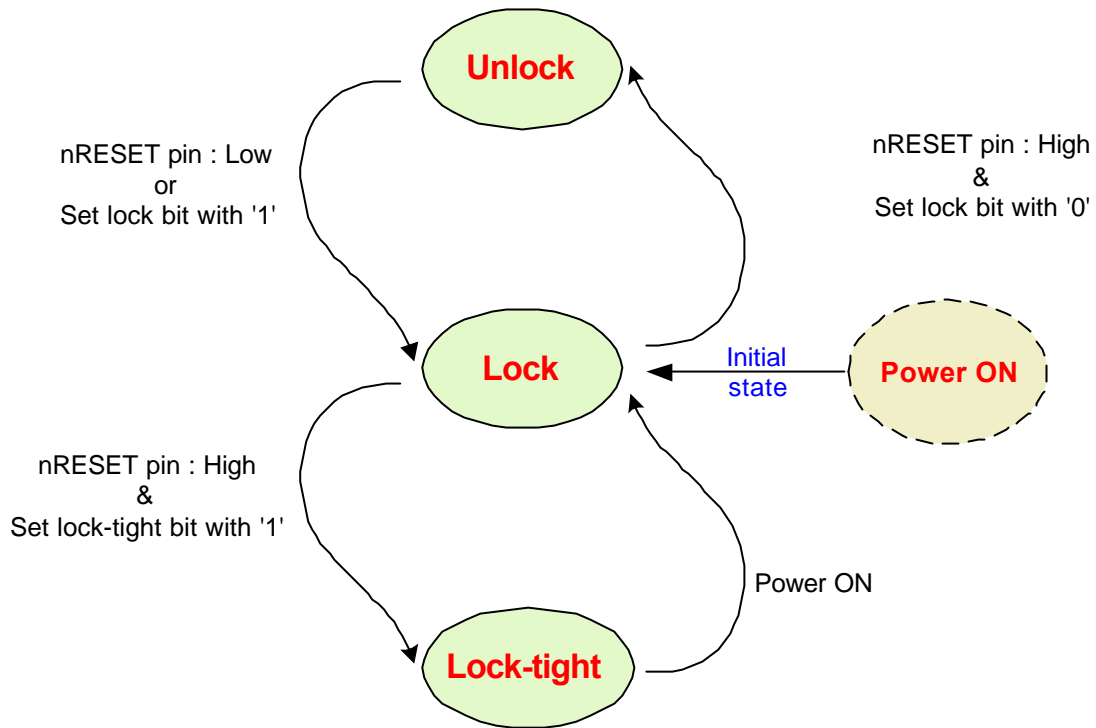
### Control Register

Register	Address	R/W	Description	Reset Value
<b>NFCNT0</b>	0x5008	R/W	Reserved	-
<b>NFCNT1</b>	0x500C	R/W	NAND Flash control register	-

NFCNT1	Bit	Description	Initial State
EnbIllegalAccINT	[4]	Illegal access interrupt control 0 : Disable interrupt                1 : Enable interrupt	0
Reserved	[3]	This bit should be '0'.	0
Reserved	[2]	This bit should be '0'.	0
EnbRnBINT	[1]	RnB status input signal transition interrupt control 0 : Disable RnB interrupt 1 : Enable RnB interrupt	0
RnB_TransMode	[0]	RnB transition detection configuration	0

NFCNT0	Bit	0 : Detect low to high                      1 : Detect high to low	Initial State
WP_En	[12]	Nand flash Write protect(fnWP) 0 : Write protect Enable(fnWP will be ' 0' ) 1 : Write protect Disable(fnWP will be ' 1' )	0
InitECC	[11]	Initialize ECC decoder/encoder(Write-only) 1 : Initialize ECC decoder/encoder	0
NFnCE	[10]	NAND Flash Memory Flash_nCE control 0 : NAND flash chip enable(Active LOW) 1 : NAND flash chip disable You must control this value in NAND Flash mode. But if HW_nCE is set to 1, also controlled by H/W.	1
Reserved	[9:4]	Reserved	000
Lock-tight	[3]	Lock-tight configuration 0: Disable lock-tight                      1: Enable lock-tight, Note: Once you set this bit to 1, you can' t clear this. In this state, you can only read.	0
Lock	[2]	Lock configuration 0: Disable lock                              1: Enable lock Note: This bit is only valid when Lock-tight bit is 0. Once you set this bit to 1, You can also read and only program the area that is determined by the block address reg.	1
MODE	[1:0]	NAND Flash controller operating mode selection 00 = Disable mode                      11 = NAND FLASH Mode NOTE: You should set one of just the above two cases.	00

**NOTE: NAND Security Block Diagram**



Note: 'Lock' can be released by S/W and 'Lock-tight' can be released only by Power ON

**Command Register**

Register	Address	R/W	Description	Reset Value
NFCMMD	0x5010	R/W	NAND Flash command set register	0x00

NFCMMD	Bit	Description	Initial State
Reserved	[15:8]	Reserved	-
NFCMMD	[7:0]	NAND Flash memory command value	0x00

**Address Register**

Register	Address	R/W	Description	Reset Value
NFADDR0	0x5014	R/W	NAND Flash address set register	-

NFADDR0	Bit	Description	Initial State
NFADDR 0	[7:0]	NAND Flash memory address value0	0x00

**Data Register**

Register	Address	R/W	Description	Reset Value
NFDATA	0x501C	R/W	NAND Flash data register	0xFFFF

NFDATA	Bit	Description	Initial State
NFDATA1	[15:8]	NAND Flash read/program data value for I/O[15:8]	0xFF
NFDATA0	[7:0]	NAND Flash read/program data value for I/O[7:0] In case of write: Programming data In case of read: Read data. These value are only used in NAND Flash mode.	0xFF

**ECC0 Register**

Register	Address	R/W	Description	Reset Value
NFECCL0	0x5020	R/W	NAND Flash ECC(Error Correction Code) register for data[7:0]	-
NFECCL1	0x5024	R/W	NAND Flash ECC(Error Correction Code) register for data[7:0]	-

NFECCL1	Bit	Description	Initial State
ECC0_2	[7:0]	ECC: Error Correction Code #2	0xXX

NFECCL0	Bit	Description	Initial State
ECC0_1	[15:8]	ECC: Error Correction Code #1	0xXX
ECC0_0	[7:0]	ECC: Error Correction Code #0	0xXX

**ECC1 Register**

Register	Address	R/W	Description	Reset Value
NFECCH0	0x5028	R/W	NAND Flash ECC(Error Correction Code) register for data[15:8]	-
NFECCH1	0x502C	R/W	NAND Flash ECC(Error Correction Code) register for data[15:8]	-

NFECCH1	Bit	Description	Initial State
ECC1_2	[7:0]	ECC: Error Correction Code #2	-

NFECCH0	Bit	Description	Initial State
ECC1_1	[15:8]	ECC: Error Correction Code #1	0xXX
ECC1_0	[7:0]	ECC: Error Correction Code #0	0xXX

Status Register

Register	Address	R/W	Description	Reset Value
Reserved	0x5030	R/W	Reserved	-
NFSTAT1	0x5034	R/W	NAND Flash operation status register	-

NFSTAT1	Bit	Description	Initial State
<b>IllegalAccess</b>	[6]	Once Lock or Lock-tight is enabled, The illegal access (program, erase .) to the memory makes this bit set. 0 : Illegal access is not detected 1 : Illegal access is detected	0
<b>RnB_TransDetect</b>	[3]	When RnB low to high transition is occurred, this value set and issue interrupt if enabled. To clear this value write ' 1' 0 : RnB transition is not detected 1 : RnB transition is detected	0
Flash_nCE	[2]	The status of Flash_nCE output pin (Read-only)	1
Reserved	[1]		
Flash_RnB	[0]	The status of Flash_RnB0 input pin (Read-only) 0 : NAND Flash memory busy 1 : NAND Flash memory ready to operate	X

NFSTAT0	Bit	Description	Initial State
Reserved	[11:0]	Reserved	0x000

**Start block address Register**

Register	Address	R/W	Description	Reset Value
NFSBLK0	0x5038	R/W	NAND Flash programmable start block address	0x000000
NFSBLK1	0x503C	R/W	NAND Flash programmable start block address	0x000000

NFSBLK1	Bit	Description	Initial State
SBLK_ADDR2	[7:0]	The 3 <sup>rd</sup> block address of the block erase operation	0x00

NFSBLK0	Bit	Description	Initial State
SBLK_ADDR1	[15:8]	The 2 <sup>nd</sup> block address of the block erase operation	0x00
SBLK_ADDR0	[7:0]	The 1 <sup>st</sup> block address of the block erase operation (Only bit [7:5] are valid)	0x00

**End block address Register**

Register	Address	R/W	Description	Reset Value
NFEBLK0	0x5040	R/W	NAND Flash programmable end block address	0x000000
NFEBLK1	0x5044	R/W	NAND Flash programmable end block address	0x000000

NFEBLK1	Bit	Description	Initial State
EBLK_ADDR2	[23:16]	The 3 <sup>rd</sup> block address of the block erase operation	0x00

NFEBLK0	Bit	Description	Initial State
EBLK_ADDR1	[15:8]	The 2 <sup>nd</sup> block address of the block erase operation	0x00
EBLK_ADDR0	[7:0]	The 1 <sup>st</sup> block address of the block erase operation (Only bit [7:5] are valid)	0x00